

Programmable Frequency Divider

The frequency divider is an important part of the frequency-synthesizer. With a programmable divider, the synthesizer's output frequency can be programmed using control digits. The programmable frequency divider can have a wide range of divide ratio. The divide ratio can be set between 2^{\min} to $(2^{\max}-1)$, where the designer can specify the min and max value. The control digits (P_0, P_1, \dots, P_n) for selecting the divide ratio are given off-chip using serial in parallel out circuits. The block diagram of the programmable divider is given in Figure 2(a). Each basic block is a divide by 2 or 3 divider. The whole circuits are composed of several blocks. The programmable divider has been simulated across various process corners, and temperature between -30°C and 70°C . Simulation results demonstrate the circuit can operate up to 5 GHz. Figure 2(b) shows the input and output signals of different blocks.

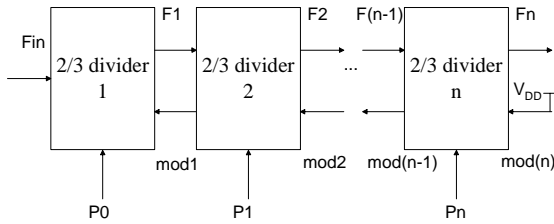


Figure 2(a) block diagram of the programmable divider

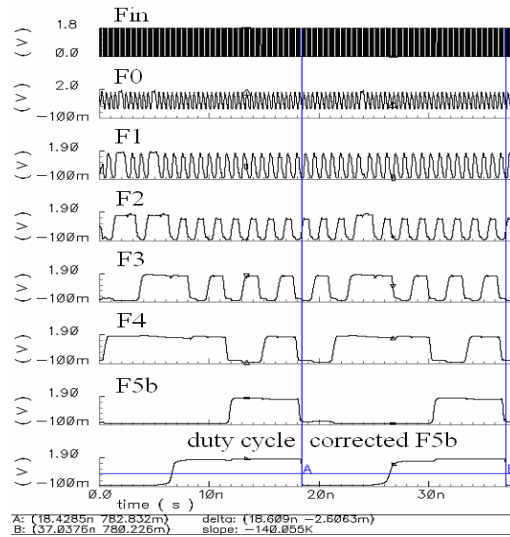


Figure 2(b) simulation results of the programmable divider

The ring VCO can generate 0~2GHz frequency with 1.8V Power supply. The divide-by-256 frequency divider can follow the ring VCO output in the entire frequency range. The programmable frequency divider works well as designed. Its dividing ration can change from 64~95. And it can also follow the entire frequency range of the ring VCO. Some testing figures are pasted below.

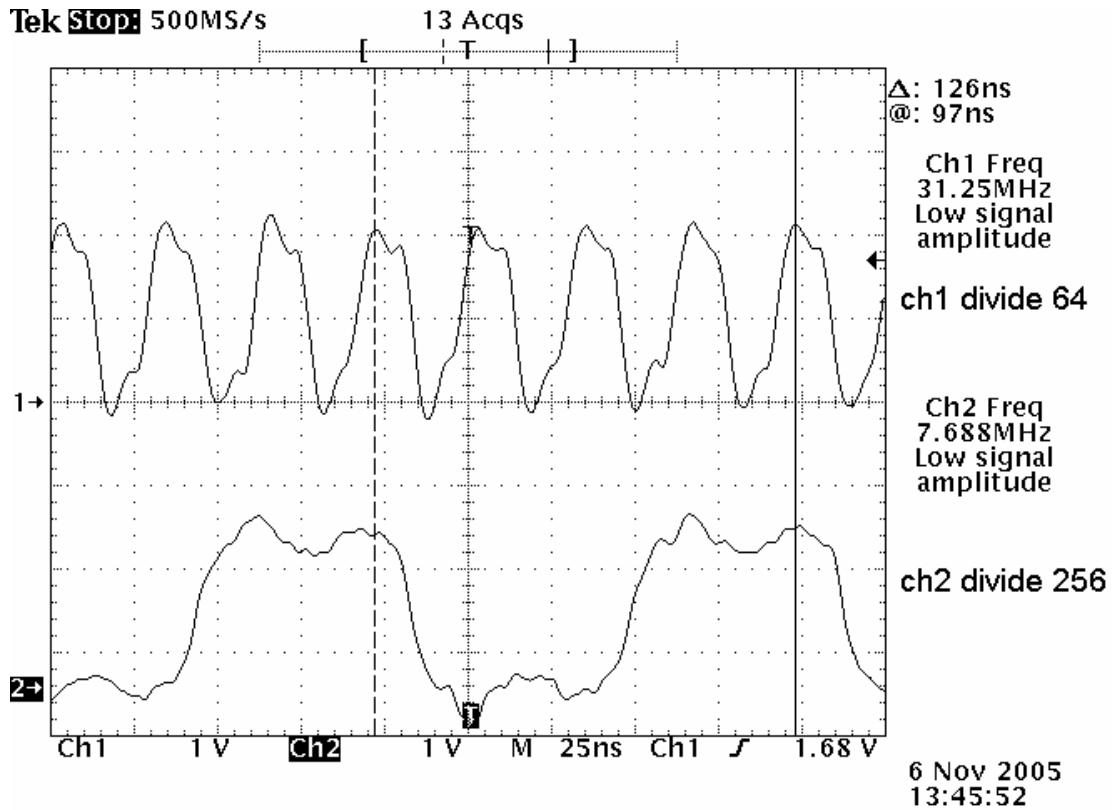


Figure---channel 1, programmable divider with dividing ratio of 64

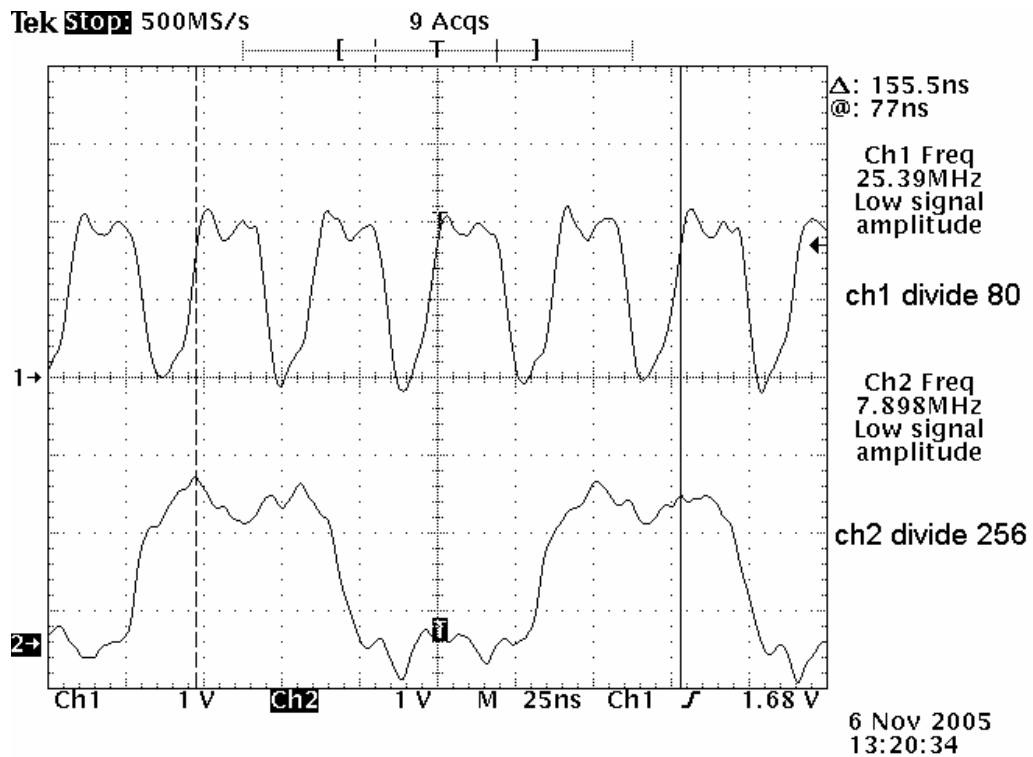


Figure---channel 1, programmable divider with dividing ratio of 80

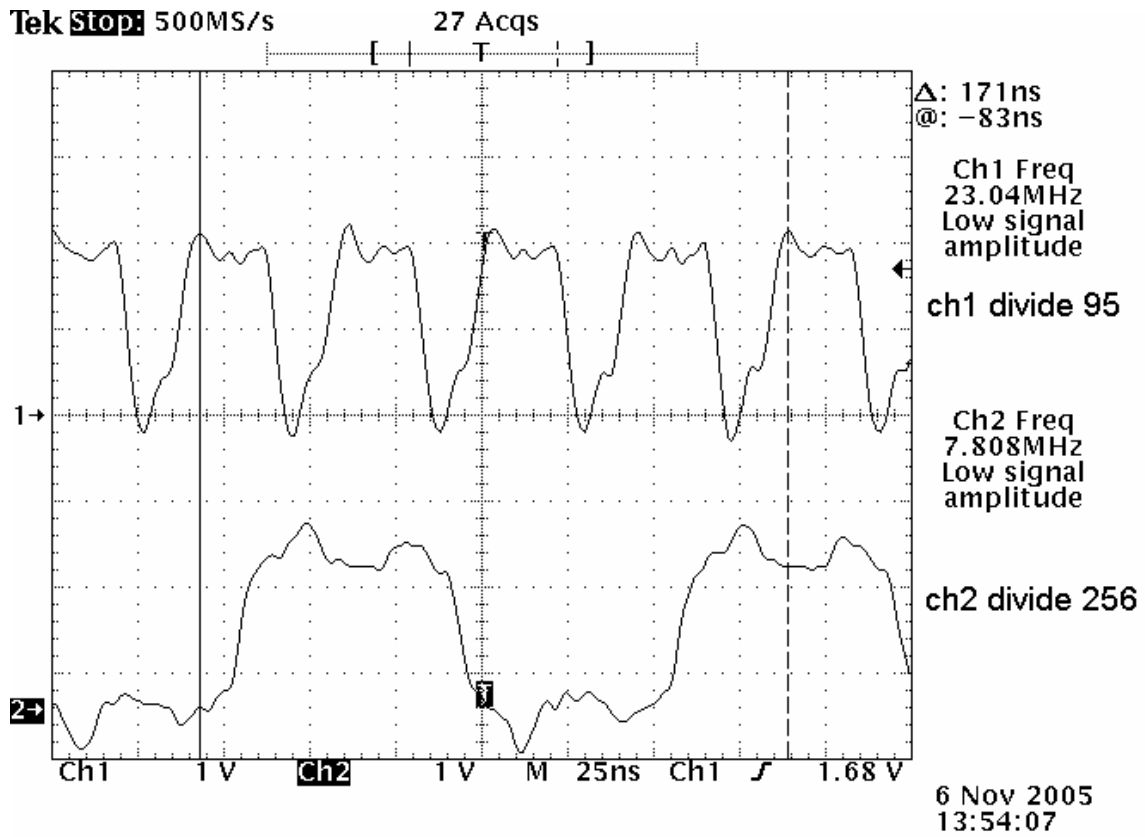


Figure---channel 1, programmable divider with dividing ratio of 95