

Design for MOSIS Educational Program (Research)

Project Title

Design of Low-Voltage RF components for realizing Fully-Integrated Zero/Low-IF Transceivers

Design NO: 71610 Fab ID:T53R-BD

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Low-power Low-noise Quadrature VCO

The Coupling transistors are used in series with the *negative-g_m* transistors. This result in lower power consumption [1]. The Q-VCO consists of two identical LC oscillators which injection lock to each other. The outputs are shown to oscillate in quadrature. The use of Both NMOS and PMOS *negative-g_m* transistors leads to dc current reuse and larger voltage swing. The table below gives a brief summary of the simulation results. Figure 1a shows the schematic and the simulation result is shown in figure 1b.

Table I: Simulation Results

Process Corner	Tuning Range (GHz)	Phase-noise @ 1-MHZ (db/c)	Power-Consumption Without buffers
Slow-Slow	1.62- 2.12	-114	8 mw
Typical	1.68-2.20	-115	11mw
Fast-Fast	1.72-2.24	-115	17mw

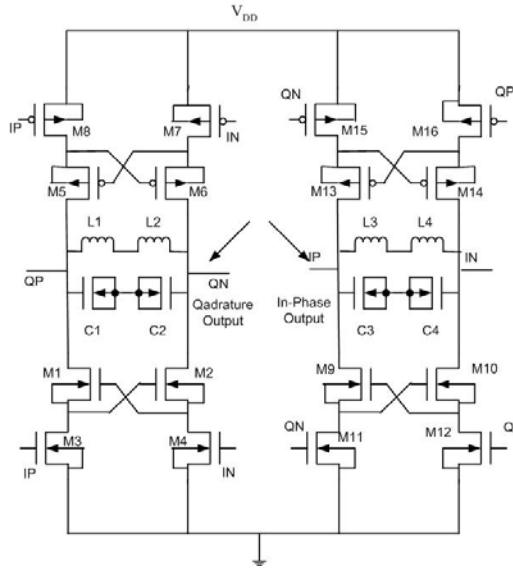


Figure 1a

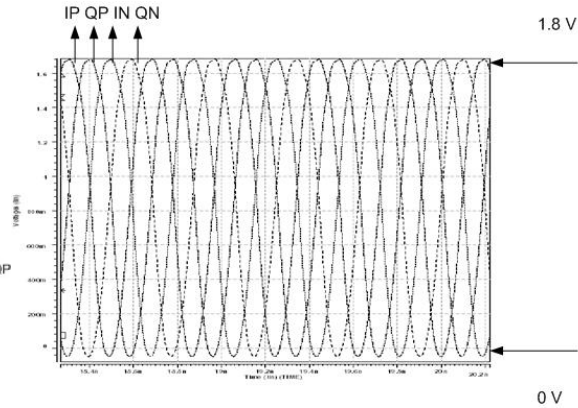


Figure 1b

An inverter based buffer is used to isolate the VCO signal from the parasitics as shown in figure 2. S-parameter simulation were carried at the output of the VCO over the frequency range of interest to build an impedance matching network to match the VCO output to the input of the Spectrum Analyzer. The simulation shows that the inverter type buffer has a large imaginary part which needs to be cancelled. Table II shows the impedance seen at the output of the buffer. Agilent ADS was used to design the matching network. Impedance matching was accomplished using microstrip transmission lines on FR4 PC board. Figure 3 and Figure 4 shows the schematic of the Impedance matching network and Figures 5 and 6 show the S11 plot of the matching networks of Figures 3 and 4 respectively.

Table II: Impedance see at the output of the buffer

Frequency (GHz)	Impedance (ohms)
1.7	41-j183
1.9	35-j163
2	32-j142
2.1	30-j138

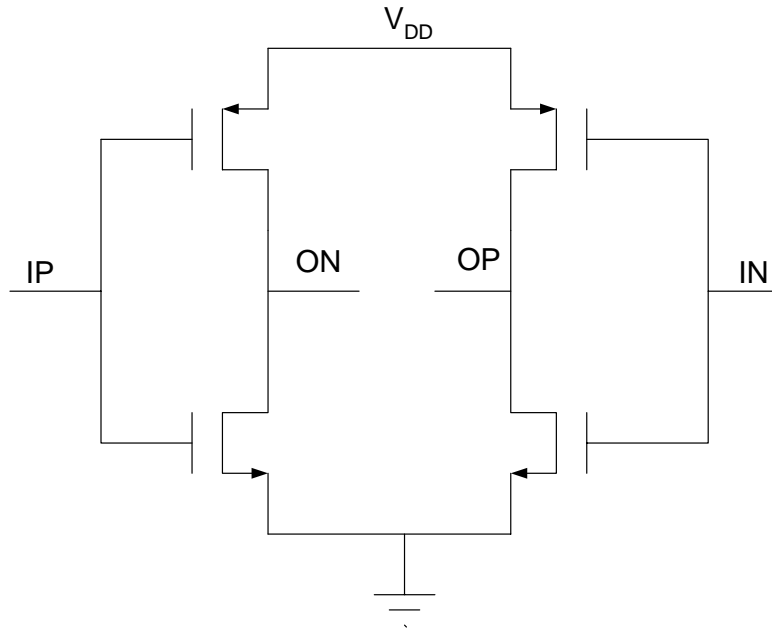


Figure 2: Inverter type buffer

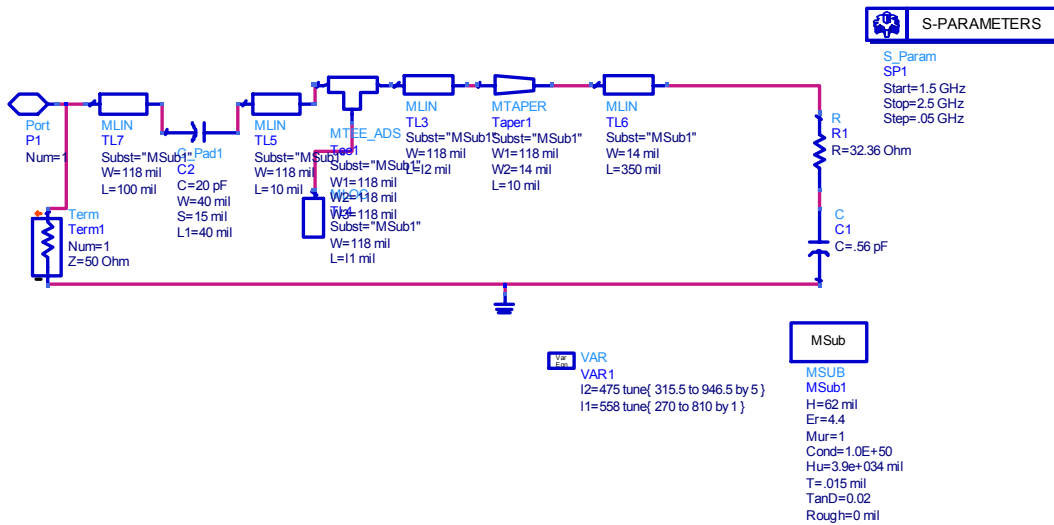


Figure 3 : Impedance matching at 2GHz

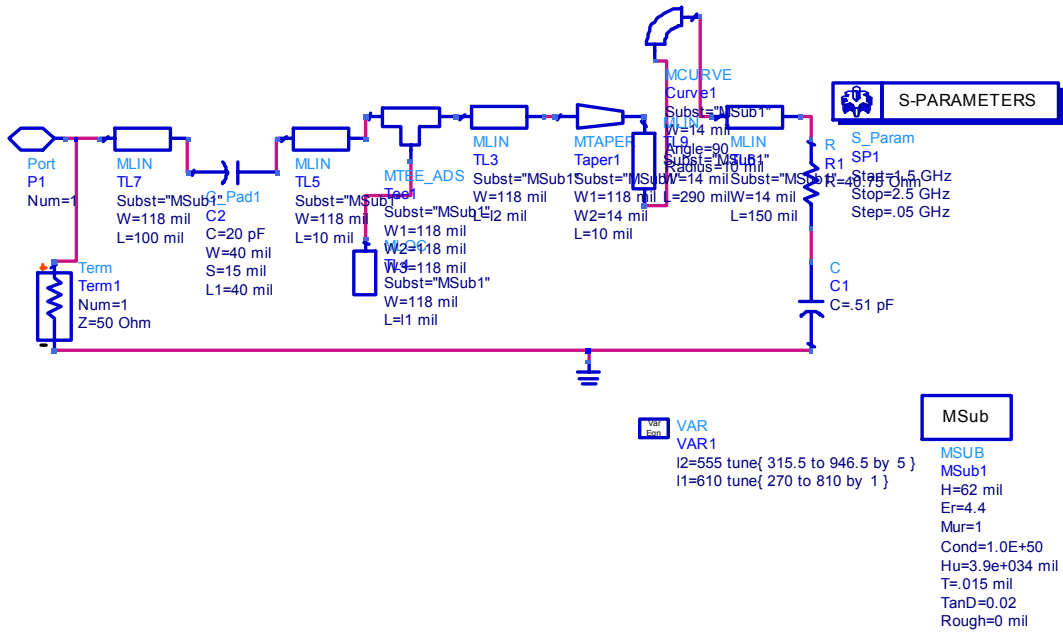


Figure 4: Impedance matching at 1.7GHz

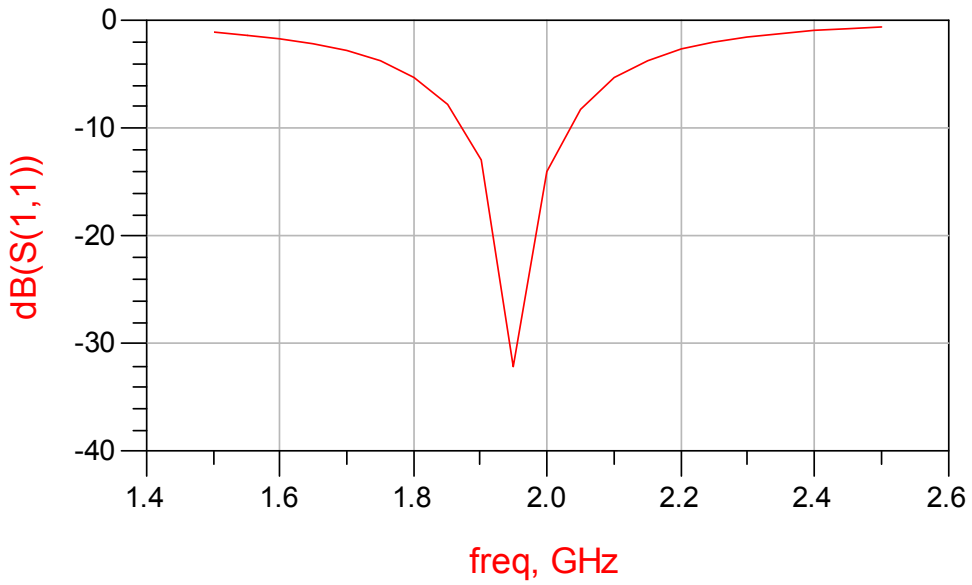


Figure 4: S11 plot of figure 3

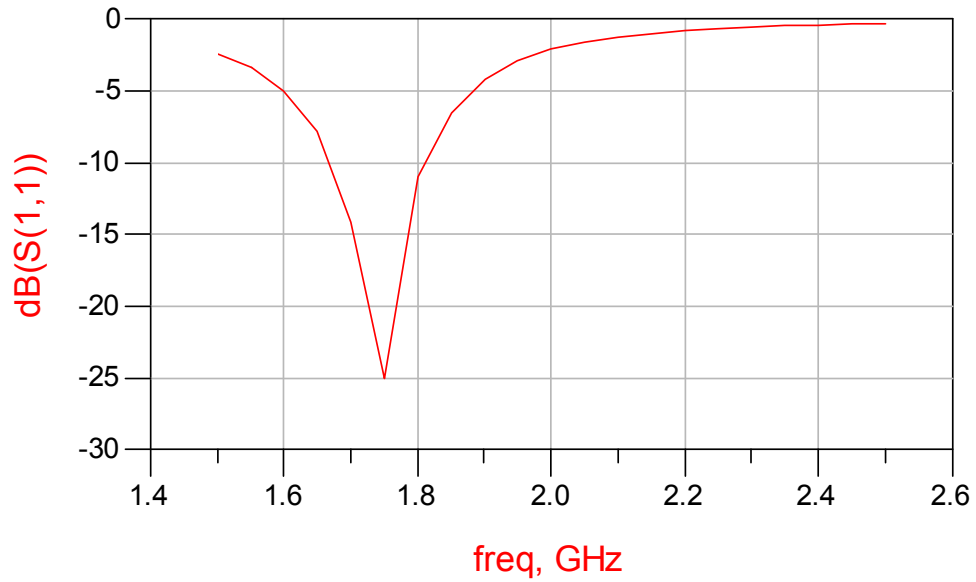


Figure 5: S11 plot of figure 4

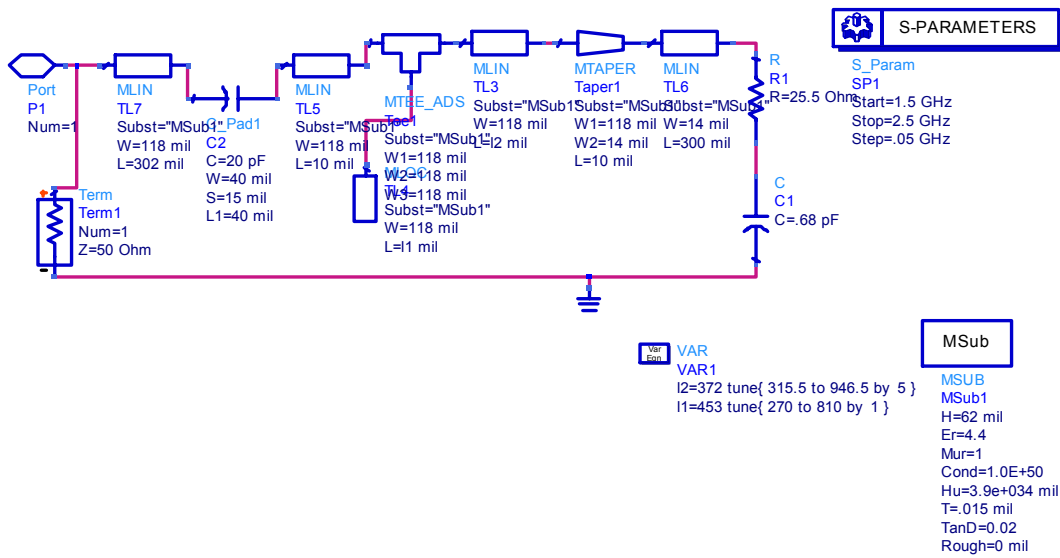


Figure 6: Schematic of matching network for 2.1GHz

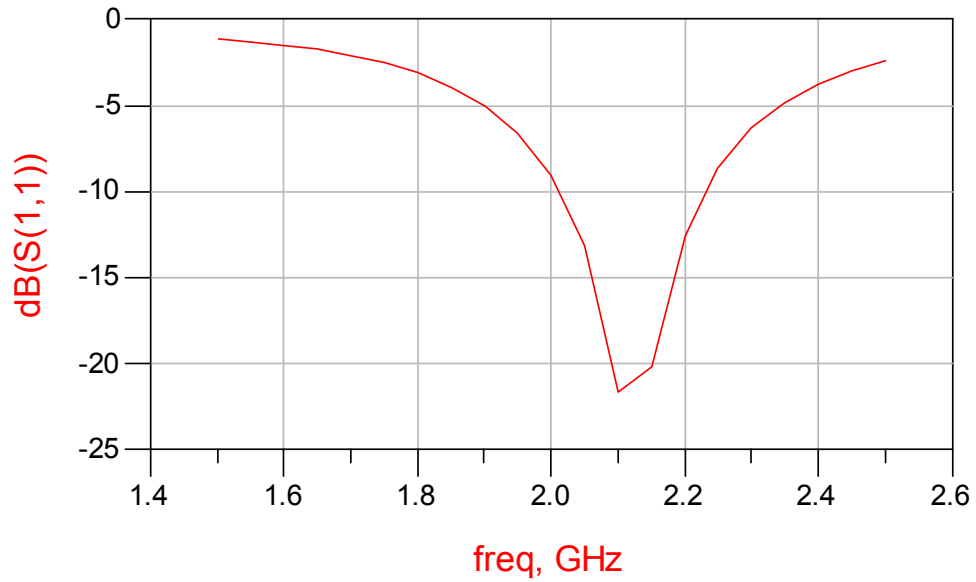


Figure 7: S11 plot of figure 6

Figure 6 achieves a S11 less than -10db for the frequency band around 1.9-2.3GHz. Since a broadband frequency match could not be achieved. A couple of different networks had to be built. Figure 8 shows the layout photograph of the VCO.

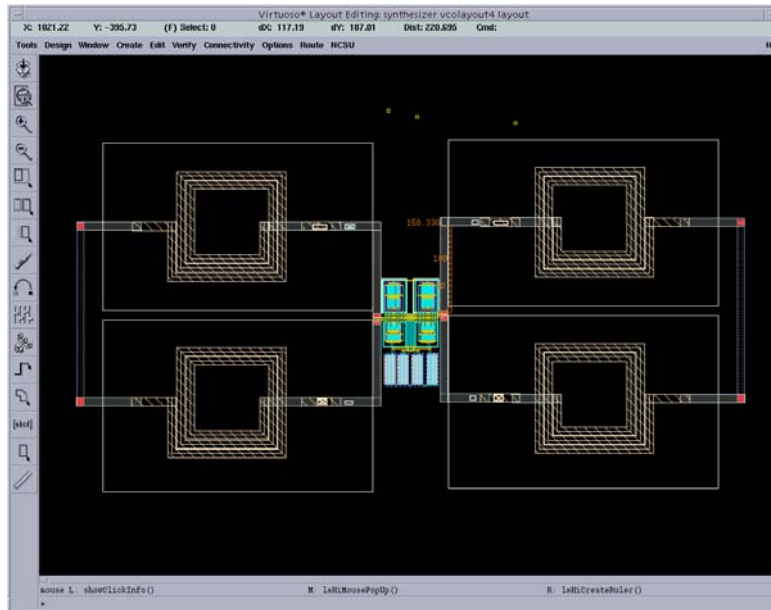


Figure 8: Layout photograph of the chip

Figure 9 shows the output of the spectrum analyzer for a control voltage of 1.8 V.

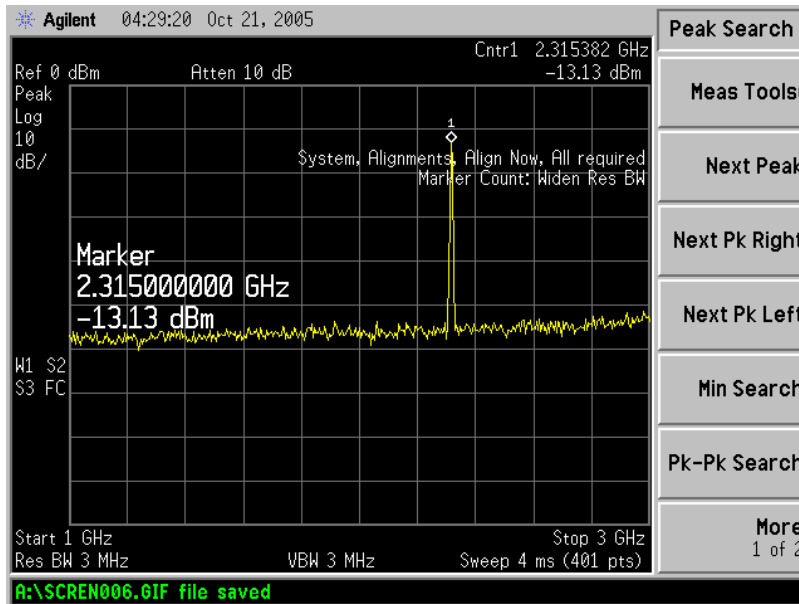


Figure 9: Output of the spectrum analyzer for $V_{cnt}=1.8V$

Simulation predicts a output frequency of 2.2GHz while the frequency measured was 2.3GHz. The VCO achieves a tuning range of .4GHz (from 1.8GHz – 2.3GHz). This is close to the simulation results. Figure 11 shows the phase noise at 1 MHz offset frequency. It is found to be -116.5 dBc/Hz which matches closely with the simulated results.

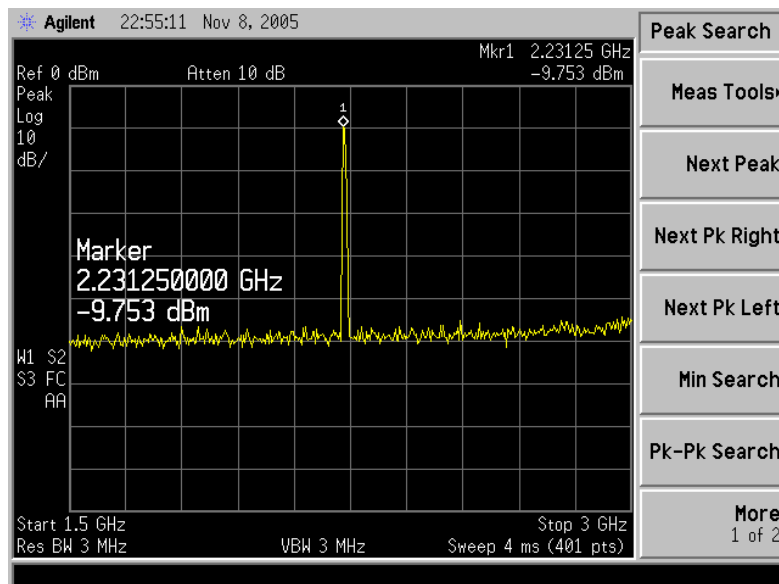


Figure 10: Output of the spectrum analyzer for $V_{cnt}=1.7V$

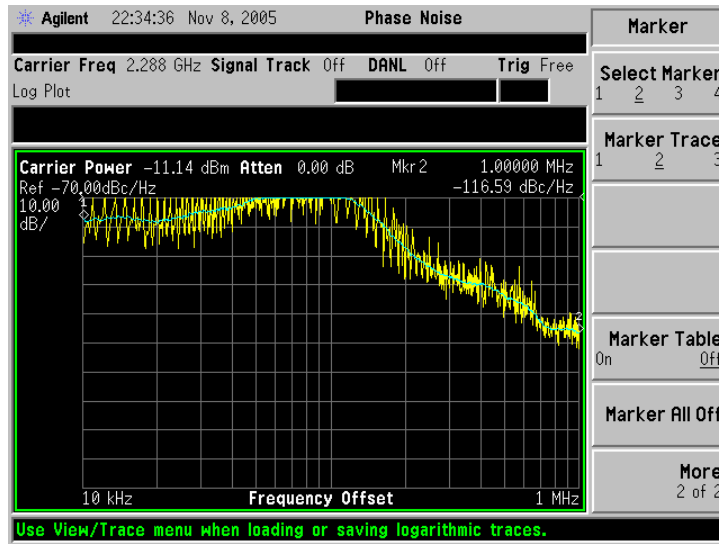


Figure 11 : Phase Noise at 1-MHZ offset frequency

Conclusion:

The measured results for the VCO matched quiet well with the simulation results. We thank MOSIS for fabricating the chip.