

## **INTRODUCTION**

This report describes the different steps of the VLSI design, simulation and performance measurement of a 4-bit counter. The particular counter I have chosen for design is a synchronous up counter with serial-carry output and input reset options. With the serial-carry output it is possible for it to be cascaded to build a counter with more bits. And the input reset pin enables the user to set the counter to 'all-zero' state and then to start it counting again from the beginning, when it is desired.

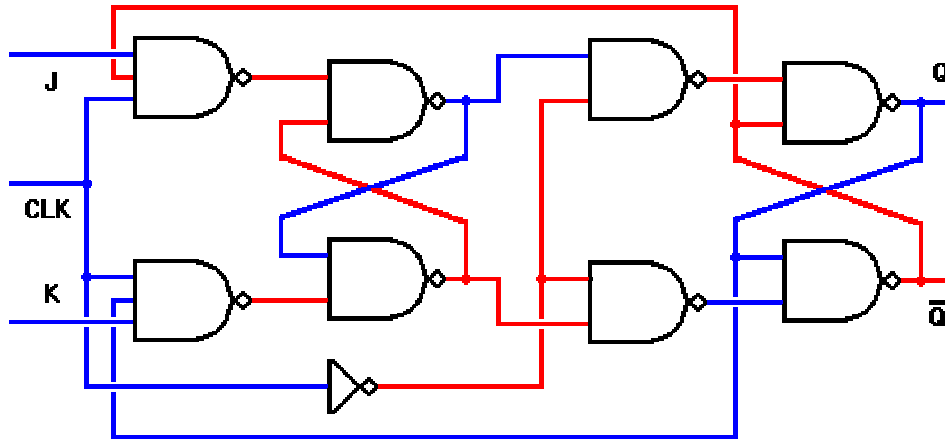
The J-K flip-flop used for this counter has been designed following a master-slave approach. Another alternative could be edge-sensitive flip-flops. However, for them to work correctly, it is necessary that the clock edges be sharp and the threshold voltage of inverters and other gates be adjusted properly. Also, the delay time through the two inverters at the input is critical. For these problems with clock and timing requirements edge-sensitive flip-flops are not good choices for IC design. Besides, the J-K flip-flop can easily be used for toggle operation and hence for counters. Therefore, the choice of the master-slave J-K flip-flop for this particular counter design has been justified.

## **THE DESIGN**

The basic building blocks of this counter are four J-K flip-flops and three AND gates. The whole design process has been described here with two steps:

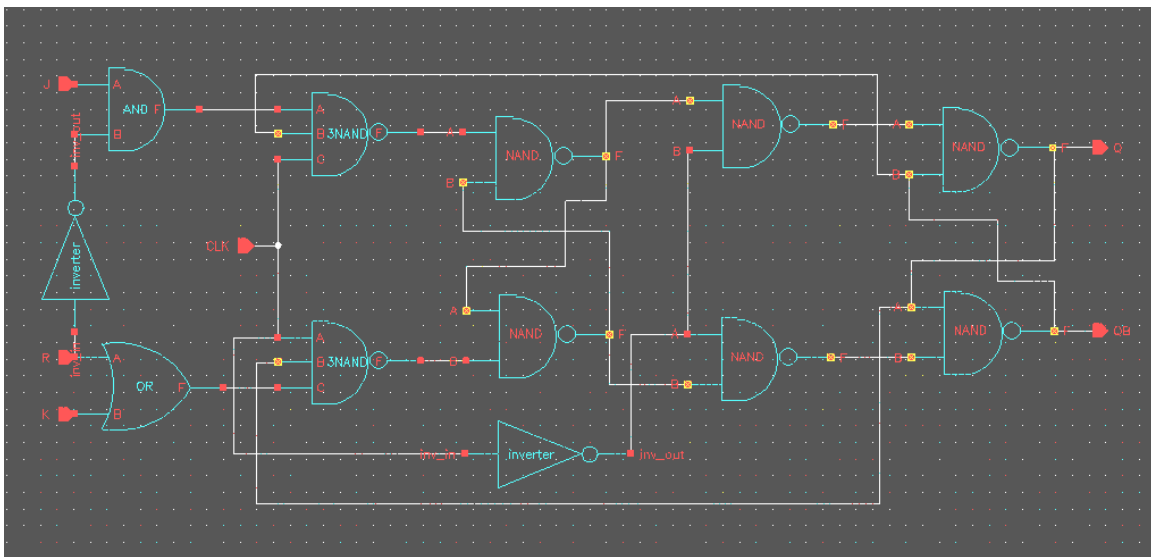
### **J-K Flip-flop**

A popular approach of designing a master-slave J-K flip-flop is using two 3-input NAND gates, six 2-input NAND gates and two inverters in a feedback loop. A change of state may occur when the flip-flop senses a negative edge of the clock signal. The logic diagram of this common design has been shown on the next page.



**Figure 1** Common Logic Diagram of a J-K Flip-flop

However, this design has been further modified to meet our specific requirement by incorporating a reset pin at the input. This has been accomplished easily by the addition of two extra gates (one AND and one OR gate) as shown in Fig. 2.



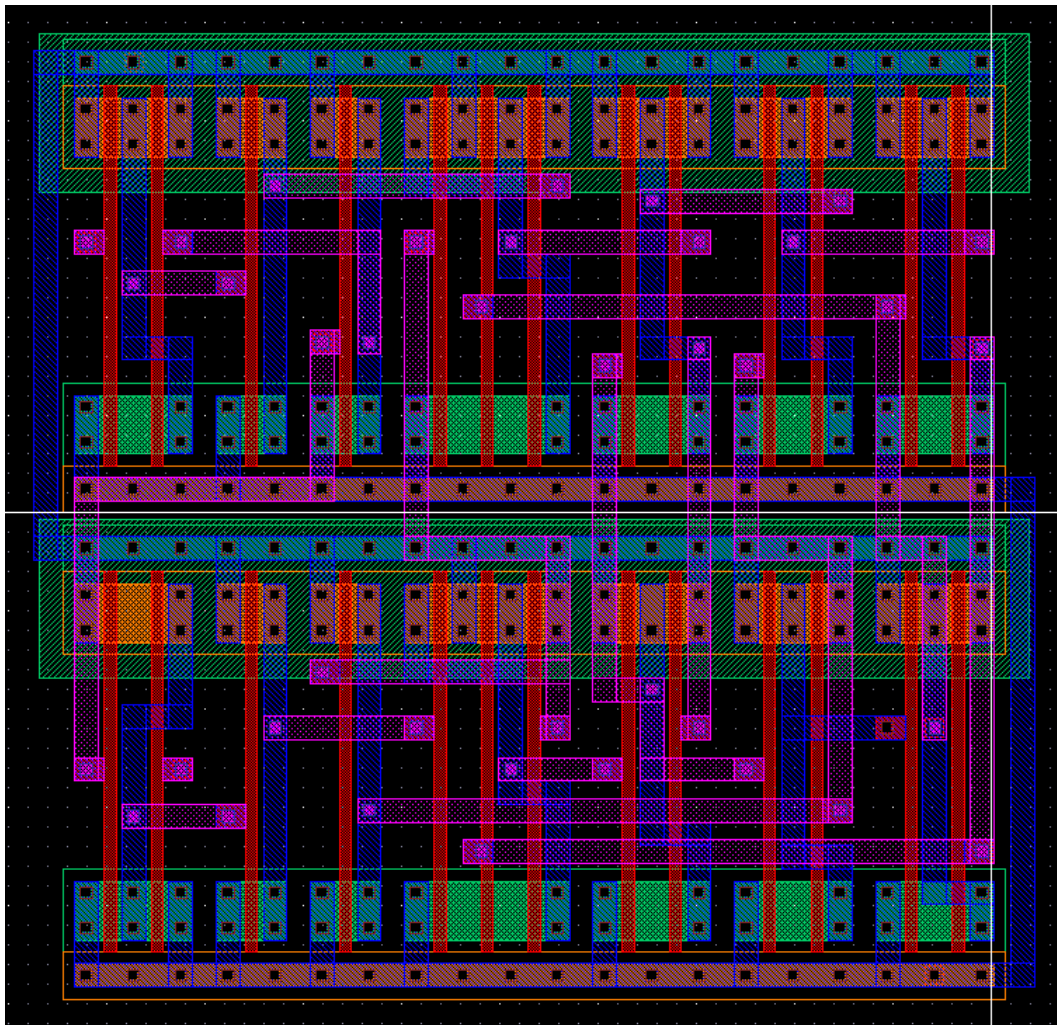
**Figure 2** Modified Logic Diagram of a J-K Flip-flop with Reset Option

When the reset input R is at logic '0', the flip-flop operates normally; whereas the output Q is forced to '0' irrespective of the input levels at J and K when R goes to '1'. Therefore, the truth table of this J-K flip-flop has been changed correspondingly:

**Table 1** Truth Table for the J-K Flip-flop with Reset

<b>R</b>	<b>J</b>	<b>K</b>	<b>Q<sub>n+1</sub></b>
0	0	0	Q <sub>n</sub>
0	0	1	0
0	1	0	1
0	1	1	$\overline{Q_n}$
1	d	d	0

After doing the layout, the J-K flip-flop looks like Fig. 3.



**Figure 3** Layout of the J-K Flip-flop in Cadence

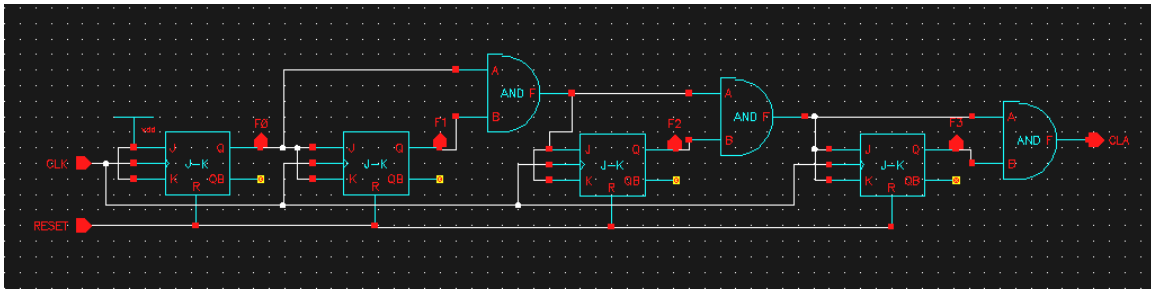
### 4-bit Counter

The following truth table shows how the 4-bit counter works along with its reset input and serial carry output. The counting states change in each negative edge of the clock pulse as long as the RESET holds a 'high' level; otherwise all the outputs are set to zero. The circuit generates a carry as all of the output bits overflow (when all outputs are '1').

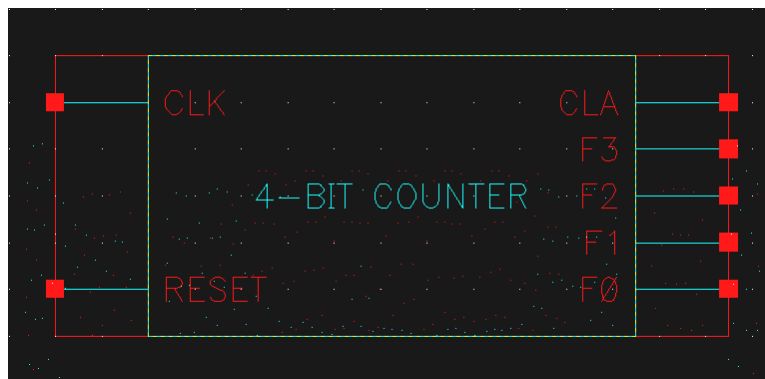
**Table 2 Truth Table of the 4-bit Counter with Reset and Carry-out**

RESET	States					Count
	CLA (carry-out)	F3	F2	F1	F0	
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
0	0	0	1	0	0	4
0	0	0	1	0	1	5
0	0	0	1	1	0	6
0	0	0	1	1	1	7
0	0	1	0	0	0	8
0	0	1	0	0	1	9
0	0	1	0	1	0	10
0	0	1	0	1	1	11
0	0	1	1	0	0	12
0	0	1	1	0	1	13
0	0	1	1	1	0	14
0	1	1	1	1	1	15
1	0	0	0	0	0	0

This counter logic has been implemented using four J-K flip-flops with their inputs shorted (for toggle operation) and some additional simple circuitry. The complete logic diagram and a symbol have been shown below:



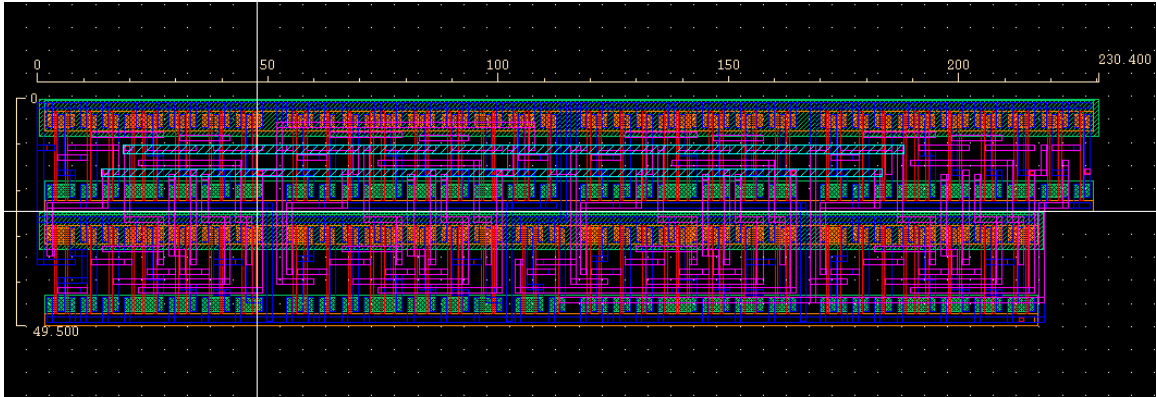
**Figure 4** Schematic for the 4-bit Synchronous Counter with Reset and Carry-out



**Figure 5** A symbol for the Designed Counter

In transistor level, the design was done using AMI 0.6 $\mu\text{m}$  process where the minimum gate length of any transistor to be 0.6 $\mu\text{m}$ . This minimum length has been adopted everywhere in the design and the width of each n-MOS and p-MOS transistor was chosen as 3.0 $\mu\text{m}$ . For simplicity the widths were kept same everywhere, and it is absolutely valid, as it does not hinder the correct functionality of the circuit and helps keeping the total chip area to a minimum. Moreover, the performance of the circuit is highly acceptable within a wide frequency range as we see from the simulation and different performance measurements.

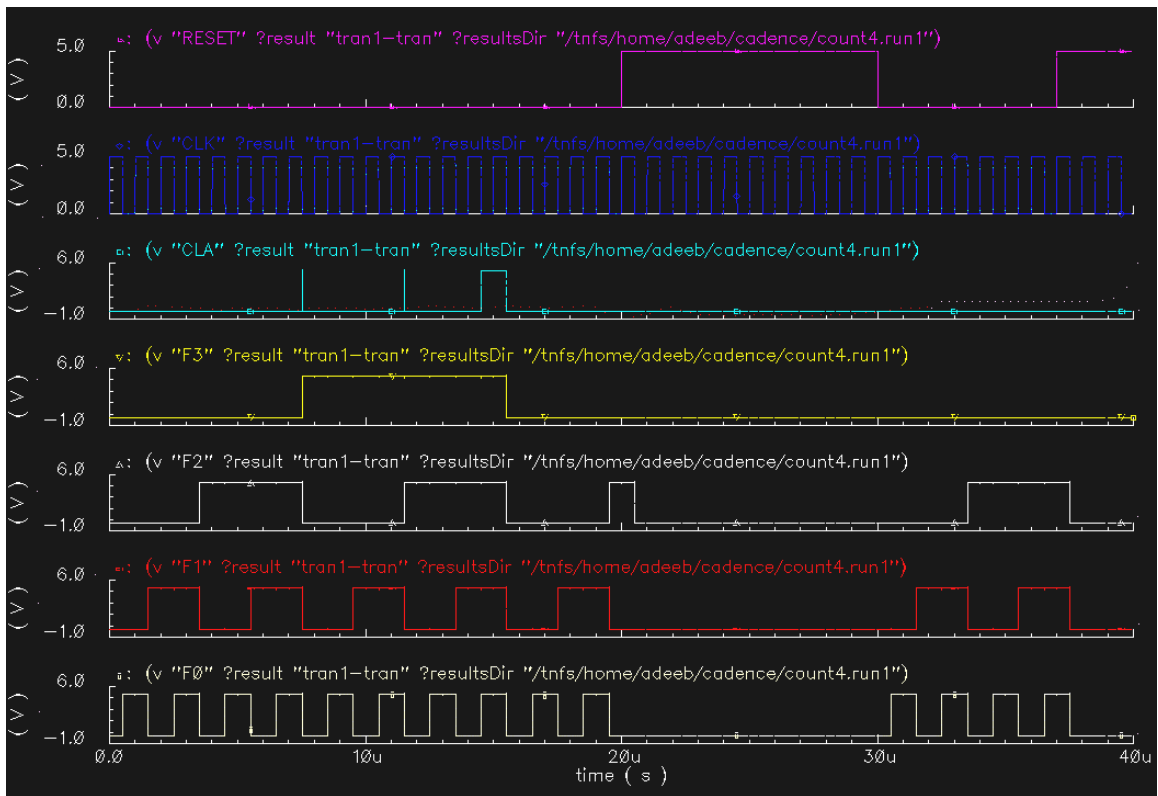
The complete layout of the 4-bit counter with all necessary interconnections is shown in Fig. 6. The active area in the layout is seen to be 230.4 $\mu\text{m}$  $\times$ 49.5 $\mu\text{m}$ .



**Figure 6** Complete Layout of the Counter

## SIMULATION RESULTS

### 1) Pre-Layout Simulation



**Figure 7** Captured Pre-layout Waveforms from Spectre Wavetool

## 2 LVS Matching

```
Text Editor - si.out
File Edit Format Options Help
@(#) $CDS: LVS version 4.4.6 03/17/2003 21:21 (cds11607) $
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /tnfs/home/adeeb/cadence/LVS/layout/netlist
count
117      nets
9        terminals
113     pmos
113     nmos

Net-list summary for /tnfs/home/adeeb/cadence/LVS/schematic/netlist
count
117      nets
9        terminals
113     pmos
113     nmos

Terminal correspondence points
1      CLA
2      CLK
3      F0
4      F1
5      F2
6      F3
7      RESET
8      gnd!
9      vdd!

The net-lists match.

                layout schematic
                instances
un-matched      0      0
rewired         0      0
size errors     0      0
pruned         0      0
active         226    226
total          226    226

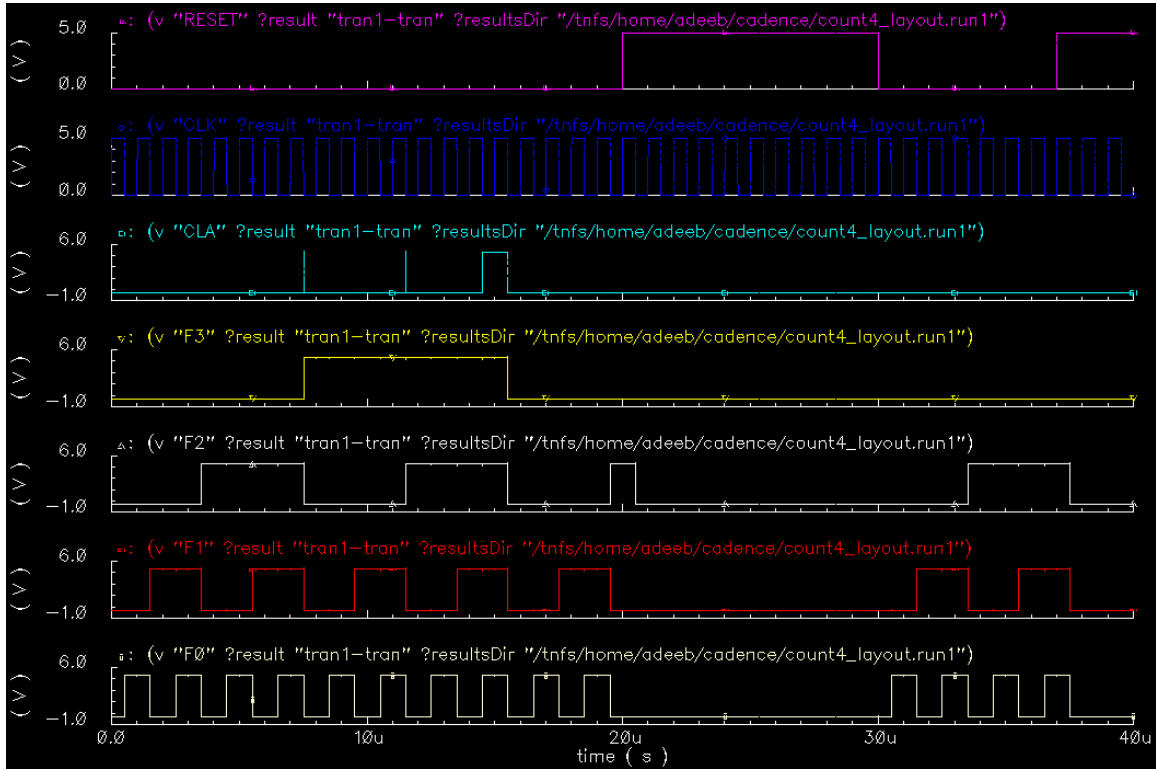
                nets
un-matched      0      0
merged         0      0
pruned         0      0
active         117    117
total          117    117

                terminals
un-matched      0      0
matched but
different type  0      0
total           9      9

Probe files from /tnfs/home/adeeb/cadence/LVS/schematic
devbad.out:
```

**Figure 8** Captured Image of the 'si.out' File (after LVS Verification)

### 3) Post-Layout Simulation



**Figure 9** Captured Post-layout Waveforms from Spectre Wavetool

### **PERFORMANCE MEASUREMENT**

A summary of several measurements regarding the performance of the designed counter is given in the following tables. All the measurements and calculations were carried out after the post-layout simulation had been done at different clock frequencies.

**Table 3 Rise and Fall Times for Different Output Bits**

Output Bit	f=1MHz		f=100MHz		f=333.33MHz	
	Rise Time (ps)	Fall Time (ps)	Rise Time (ps)	Fall Time (ps)	Rise Time (ps)	Fall Time (ps)
F0	316.43	256.831	325.261	255.676	324.555	255.512
F1	192.856	144.435	186.274	144.445	186.519	144.022
F2	202.729	151.865	196.78	152.239	195.551	152.383
F3	192.779	144.724	185.265	144.25	185.817	144.461

**[Comments:**

- The rise time or fall time does not depend on the frequency of operation. The little discrepancies might have occurred due to error in measurement.
- The fall time for each bit is less than the rise time for that bit. It means the discharging RC constant is less than that of the charging one.
- The rise and fall times are calculated using a 30%-70% method.]

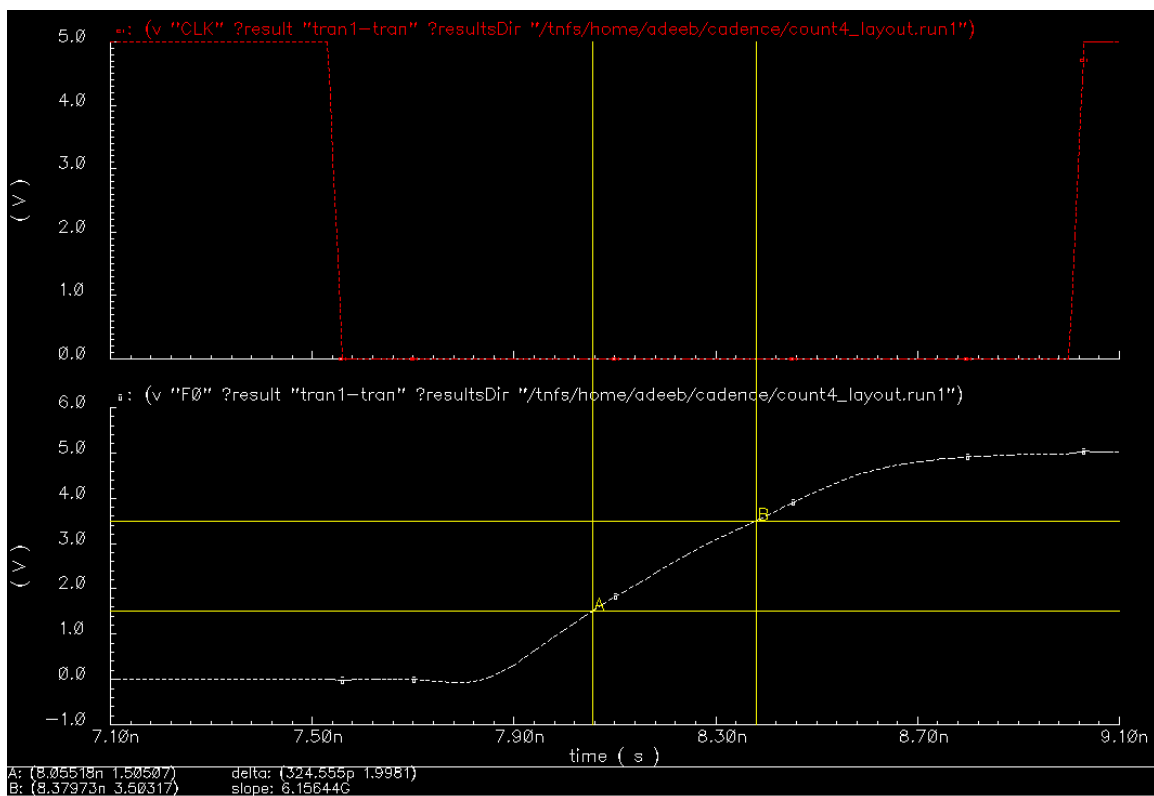
**Table 3 Propagation Delay Times for Different Output Bits**

Output Bit	C <sub>L</sub> =0		C <sub>L</sub> =10fF		C <sub>L</sub> =30fF		C <sub>L</sub> =50fF	
	Delay: '0' to '1' (ps)	Delay: '1' to '0' (ps)	Delay: '0' to '1' (ps)	Delay: '1' to '0' (ps)	Delay: '0' to '1' (ps)	Delay: '1' to '0' (ps)	Delay: '0' to '1' (ps)	Delay: '1' to '0' (ps)
F0	814.34	922.429	874.499	976.168	994.319	1085	1112	1193
F1	608.787	771.935	673.324	827.619	799.851	937.104	920.208	1045
F2	624.721	786.465	690.302	841.3	816.031	950.339	936.094	1058
F3	607.029	773.691	673.639	829.267	800.638	937.815	922.315	1046

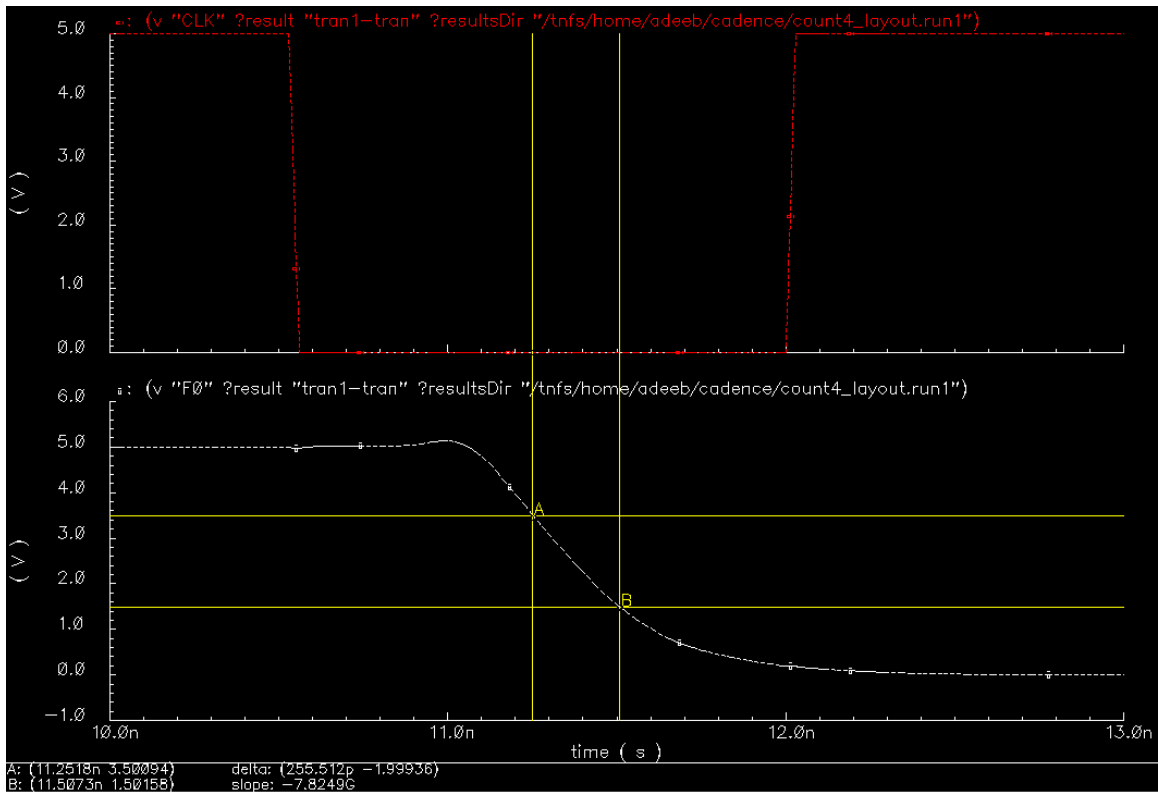
**[Comments:**

- The delay time for the counter increases as the load capacitance increases before the output waveforms become distorted with a load of about 80fF.
- The delay times for '1' to '0' transitions are greater for each bit at every load than those for '0' to '1' transitions.
- Measurements for the delay times are done using a 30%-70% method.

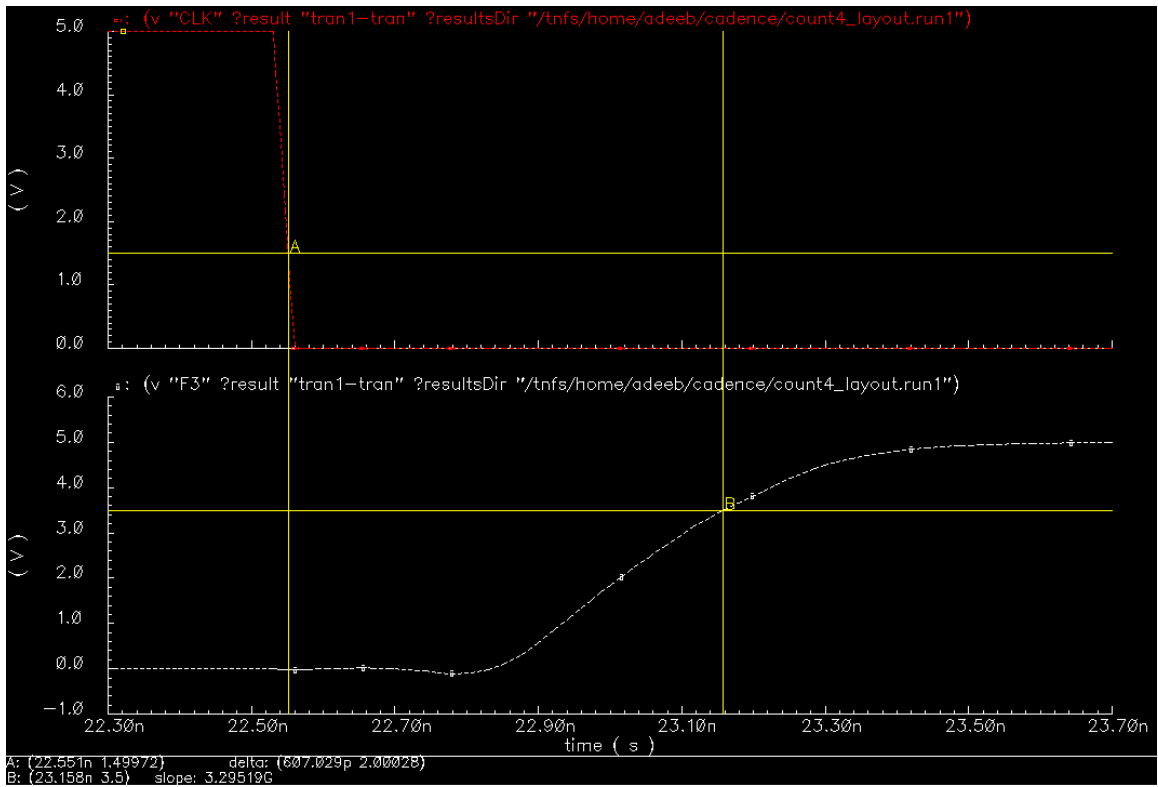
Some captured images of these performance measurements have been attached herein.



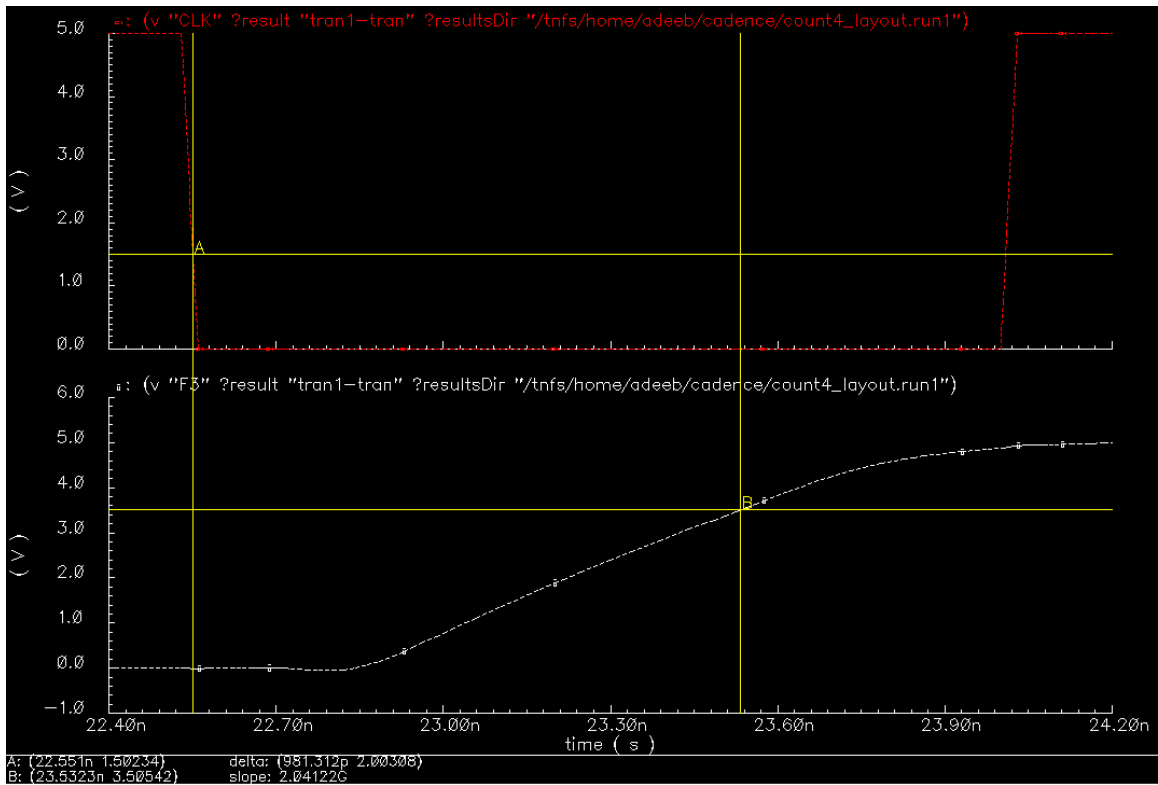
**Figure 10** Rise Time Measurement for the LSB at 333MHz



**Figure 11** Fall Time Measurement for the LSB at 333MHz



**Figure 11** Propagation Delay Measurement for the MSB at 333MHz without Load



## **Figure 12** Propagation Delay Measurement for the MSB at 333MHz with 60fF Load

### **SUMMARY**

From all the discussions above we can summarize the salient features of the designed counter as follows:

- ▶ 4-bit Up Counter
- ▶ Asynchronous Reset Input ('0' for normal operation, '1' for reset)
- ▶ Serial Carry-out
- ▶ Maximum Clock Frequency: approx. 350MHz
- ▶ Maximum Rise Time @ 333MHz: 325ps (for a clock with 1% rise and fall time)
- ▶ Maximum Fall Time @ 333MHz: 256ps
- ▶ Maximum Propagation Delay without Load @ 333MHz: 922ps
- ▶ Maximum Capacitive Load before Distortion @ 333MHz: 60fF
- ▶ Active area of the Layout: 0.0114mm<sup>2</sup> (230.4mm'49.5mm)
- ▶ Process: AMI 0.60mm
- ▶ Supply Voltage: 5V

### **APPLICATIONS**

Digital counters have numerous applications in modern electronic technology. Only a few of them have been mentioned here:

- As a frequency divider in phase-locked loops or frequency synthesizers used in very high-speed communication systems
- In digital clock and timing circuits
- Microcontrollers and digital memories
- Display drivers
- Measurement circuits
- Signal generation and processing circuits

- Consumer electronics

## **CONCLUSION**

This project has given us an opportunity to exercise our skills in designing (both schematics and layouts) digital VLSI circuits with the help of the state-of-the-art Custom IC Design Tools, Cadence. From the different design steps we have learned about digital circuit design techniques, proper choice of transistor sizes, design rules, laying out the circuit with minimum possible area, pre and post layout simulation (with Spectre), layout extraction, LVS matching and measurement of different performance factors. This project should be considered a successful one as it ends up with a working circuit that exhibits satisfactory performance in the simulation results.