

Design for MOSIS Educational Program (Research)

Project Title

Design of Programmable Electron Counter for Charge Sensing Applications

Fabrication Report

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Fab-ID: T54GAW

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Project Description

The field of nanotechnology enforced strict limitations on the size and the operating signal levels of the sensors and transducers. Hence most of the sensors either operate with extremely low charges or their equivalent current levels. These sensors are extremely versatile and they find themselves in a wide variety of applications. Hence precise operation of these sensors operating at such extremely low charge levels demanded the development of new control circuits. The control circuits should be based on a fixed dose (charge-level) as opposed to fixed current-levels. A novel circuit called the Electron Counter (E-Counter) [1] is capable of sensing charges by counting the desired number of electrons and producing appropriate control signal when the desired amount of charge is emitted. The E-Counter presented in [1] was capable of counting $15e6$ electrons from current levels in the range of nano-amperes. In the current work, the E-Counter will be modified to obtain a variable electron count. This is accomplished by varying the integrating capacitor rather than having a fixed capacitor

Figure 1 shows the functional schematic of the E-Counter [1] that can achieve a fixed count of $15e6$ electrons. The Count_Start is the only input control signal to the E-Counter. When the Count_Start signal is "OFF", the integrator operates in unity-gain feedback configuration and output of the integrator (V_{INT}) is set to a reference voltage (V_{REF2}). When the Count_Start signal is "ON", the operational amplifier operates as an integrator and the charge is accumulated from the Q_{SENS} , onto the C_{INT} . A poly2-poly1 capacitor is used for the integration capacitance, which linearly transforms the charge given the sensor into voltage (V_{INT}) by the following equation:

$$dQ = C * \delta V \quad (1)$$

where dQ represents the total charge given by the sensor, C indicates the integration capacitance and δV indicates the voltage equivalent of the accumulated charge.

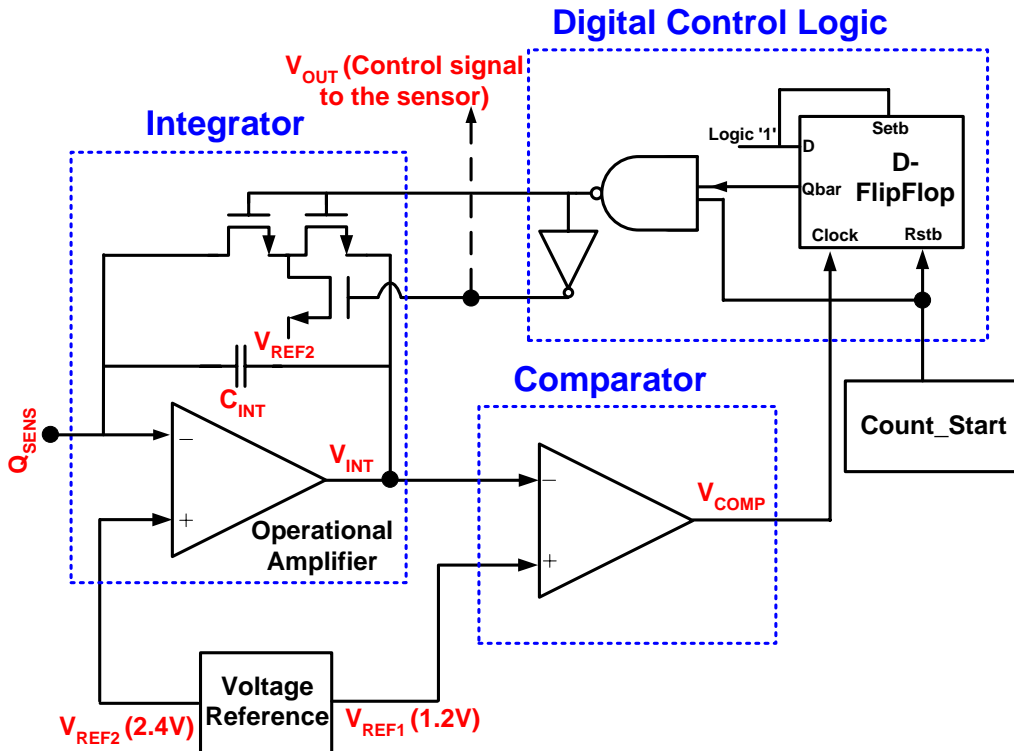


Figure 1 Schematic of the E-Counter

The total charge corresponding to $15 \times e^6$ electrons can be calculated as:

$$dQ = 15 \times 10^6 \times 1.6 \times 10^{-19} \text{ Coulombs}$$

$$\Rightarrow 24 \times 10^{-13} \text{ Coulombs}$$

Assuming this charge is given by a 1nA current source, the charge is converted into current by the following equation:

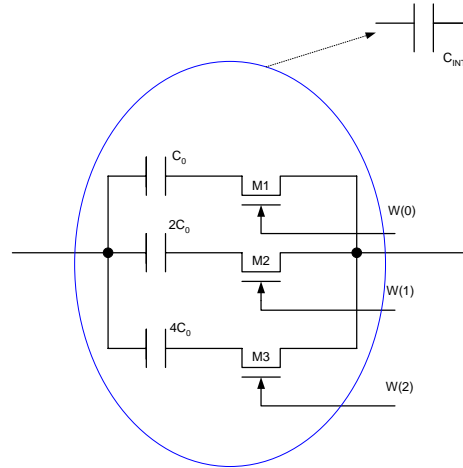
$$i = \frac{dQ}{dt} \quad (2)$$

The time taken by a 1nA current source to deliver 24×10^{-13} coulombs is calculated to be 2400 μ s. As explained earlier, V_{INT} is set to V_{REF2} , before the sensor starts emitting the charge. The Integrator is designed in such a way that V_{INT} reaches V_{REF1} , when the desired amount of charge is accumulated on the C_{INT} . The charge given by the Q_{SENS} is converted into voltage by the integrator, when the Count_Start is asserted "HIGH". The charge to voltage conversion has a linear relationship given by:

$$i(t) * dt = C * dV \quad (3)$$

Where: $i(t)$ denotes the current equivalent of the charge emitted by the sensor, C indicates the integration capacitance, dv shows the voltage difference between start and the end of the integration process and dt indicates the duration of integration. In this design, dv is fixed to 1.2V, which is conveniently generated by the difference between two on-chip reference voltages V_{REF1} and V_{REF2} . These reference voltages are generated using a bandgap reference circuit and a voltage doubler. From equation (3), the capacitance was calculated to be 1.92pF for counting $15 \times e^6$ electrons. Since the integration capacitance (C) and the difference in the voltage (dv) are constant in the above equation, dt adapts itself according to the current $i(t)$, such that the product $i(t)*dt$ remains constant. To summarize, it takes 2400 μ s to count $15 \times e^6$ electrons using an integration capacitance of 1.92pF, assuming the desired charge is supplied by a constant current source of 1nA. If the current level varies, dt would adapt accordingly, to count the desired number of electrons.

To obtain a programmable electron count the capacitor C_{INT} shown in Fig 1 is made a variable capacitor. Binary weighted poly1-poly2 capacitor and NMOS switches whose widths are binary weighted constitute variable capacitor. This type of an arrangement offers an effective capacitance that is highly linear. Figure 2 shows the variable capacitor formed by binary weighted capacitors C_0 , $2C_0$ and $4C_0$, where C_0 is 100fF. Thus, the capacitance can be varied linearly from 100fF to 700fF by varying the 3-bit control word $W(0:2)$ from 001 to 111. With the dv and current fixed at 1.25v and 1nA respectively in (3), it is theoretically possible to achieve electron counts from $9e5$ to $6.25e6$.



The integrator block primarily uses an operational transconductance amplifier (OTA) and a feedback capacitor for implementing the desired integrator. Initially, the switch in the feedback loop is closed by the digital control logic and the OTA operates in unity-gain feedback configuration. This not only ensures the proper biasing of the OTA but also initialized V_{INT} to V_{REF2} . When the Count_Start signal goes "HIGH", the switch opens and OTA operates as an integrator.

A folded cascade configuration has been chosen for achieving the high gain and a good phase-margin. The high gain of the OTA not only helps reducing the systematic gain error, but also reduces the impact of parasitic capacitance at the input node. The comparator is implemented as in [2]. The comparator consists of a pre-amplification and decision circuits with low propagation delay. The propagation delay and the offset of the comparator are of prime importance since they contribute directly to the error in the electron count. The propagation delay of the comparator and the digital control logic from the integrated system was simulated to be approx. 13ns, which is negligible ($\ll 0.001\%$) compared to the total integration time.

A digital logic consisting of a D-Flip-flop, NAND gate and an inverter is referred as the digital control logic and is shown in Figure 4. The signal $V_{SWITCH_}$, an inverted version of the V_{SWITCH} is used for controlling the E-Counter (shown in the Figure 4) i.e., when Count_Start is “OFF”, $V_{SWITCH_}$ is also “OFF”. Hence the feedback switch is closed and the E-Counter will not count any electrons. When Count_Start turns “ON”, $V_{SWITCH_}$ is turned “ON”, thereby starting the count process. The rising edge generated by the V_{COMP} acts as the clock to the D-Flip-flop, which turns “OFF” the Qbar, thus turning “OFF” the $V_{SWITCH_}$. This stops the electron counting process. The propagation delay of the digital control logic does not cause any error in the electron counting process, since the propagation delay during the start of the integration process is cancelled by the propagation delay during the termination of the integration process(after the V_{COMP} turns “ON”). The signal V_{SWITCH} is used to control the feedback control switch, which indicates the start/end of the integration process. When the Count_Start signal is “OFF”, D-Flip-flop stays in reset state, and $V_{SWITCH_}$ is “OFF”.

Test Results from the Fabricated Chip and Comparison with Simulation:

The simulation is performed using Hspice with the models for AMI 0.5 μ process available in MOSIS website. The simulation results for various capacitance values are given in Table 1 along with the measured values. The Waveforms are shown for a capacitance of 500fF in figure 3. A current of 5nA was used for testing the system as the results were found to be more accurate for currents greater than 5nA.

Integration Capacitor (W(0:2))	dt (μ s) - Simulated	dt (μ s) – Tested	Electron Count from simulation	Electron Count from Test Results
100(001)	30	55	.93e6	1.71e6
200(010)	52	70	1.62e6	2.18e6
300(011)	75	87	2.34e6	2.71e6
400(100)	100	109	3.12e6	3.4e6
500(101)	125	131	3.9e6	4e6
600(110)	150	157	4.68e6	4.9e6
700(111)	175	178	5.46e6	5.56e6

Table 1: Test Results VS Simulated Results for Values for Different Integration Capacitances

As shown in the above table the error between the simulated and tested results match well for a capacitance greater than 400fF. This is due to the fact that for lower capacitance parasitic capacitance is significant.

Current	Chip 1	Chip 2	Chip 3
2 nA	10%	14%	12%

5 nA	4%	1%	1%
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Table 2: Test Results showing the accuracy of electron count across 3 different chips for a capacitance of 500fF

Table 2 show the test Results from CMOS E-Counter shows that the error between the theoretical and experimental results (time to sense a given amount of charge). Results indicate that the system is accurate for higher currents. A Keithly 2400 source meter supplies the input current (for test purposes). Part of the error is attributed to input current fluctuation. Figure 2 shows the test results for a capacitance of 500fF.

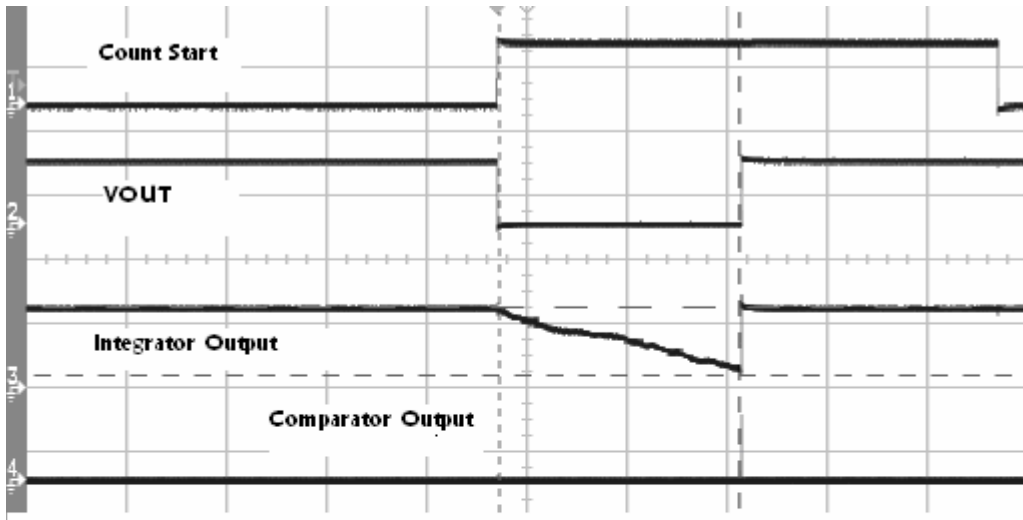


Figure 2: Test Results for C= 500Ff

Conclusion:

The chip was tested successfully and it was found that the system was accurate for a current more than 5nA and a capacitance more than 400fF.

Acknowledgements:

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