

**DESIGN FOR MOSIS EDUCATIONAL PROGRAM
(Research)**

T3BM-AC

Project Title

**A 1.8 GHz CMOS VCO employing On-Chip Inductors and
Body-Driven Varactors**

Prepared By: Lakshmipriya Shesan and Dr. Syed Islam

**Institution: EE Department, University of Tennessee,
Knoxville**

Introduction

This aim of this project was to design RF VCOs employing On-chip Inductors in TSMC 0.35 μ technology. This was the first project at the University of Tennessee that used On-chip Inductors. The Inductor models were not available. Therefore, ASITIC was used to model the inductors. Thus the purpose of this project was to employ on-chip inductors successfully for RF circuit design and to compare the simulation and the test results. The authors would like to thank MOSIS for fabricating their design.

Project Description:

The schematic of the LC-VCO is shown in figure 1. The Pi- model for the inductors shown in figure 2 was used for schematic simulation. The Pi model is extracted using ASITIC. It models the losses associated with the On-Chip Inductors. The Inductor used was an Octagonal shaped fully symmetric Inductor. The layout of the Inductor is shown in Figure 2. The advantage of using such an inductor is its high quality factor compared to the single ended Inductors. The Varactor used was a body-driven Varactor with the source and drain grounded and the body connected to the control voltage. This gives a monotonic variation of capacitance with the control voltage and also a high tuning range. The Varactor operates in accumulation and depletion modes.

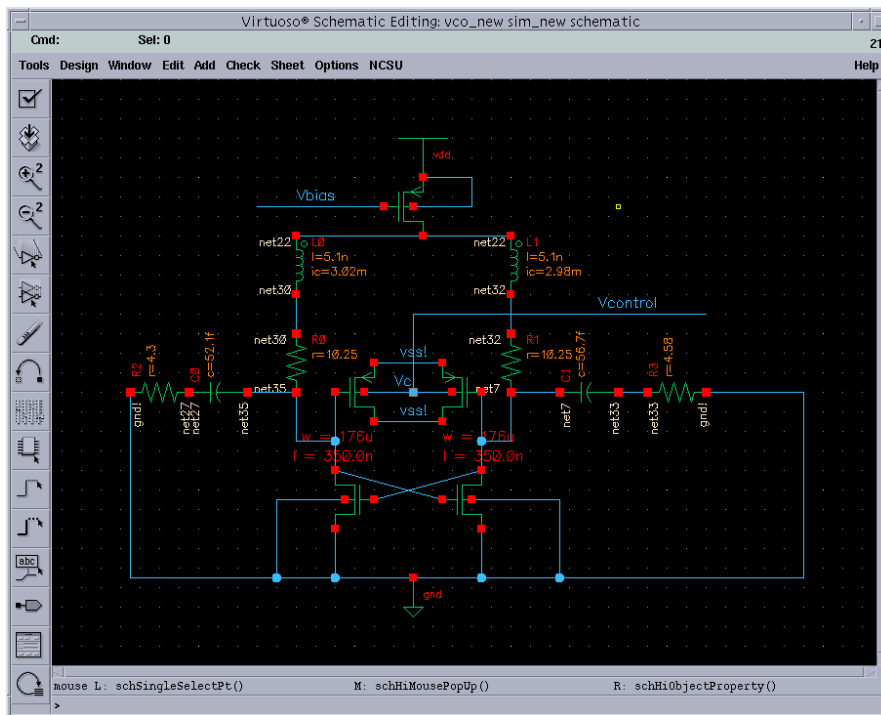


Figure 1: Schematic of the LC VCO

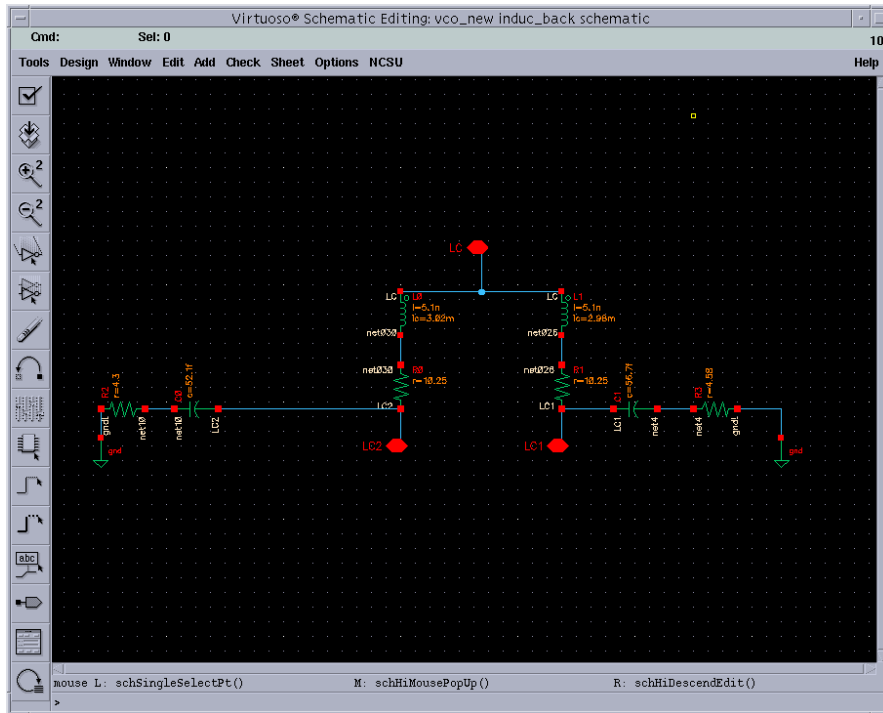


Figure 2: PI Model of the Inductor

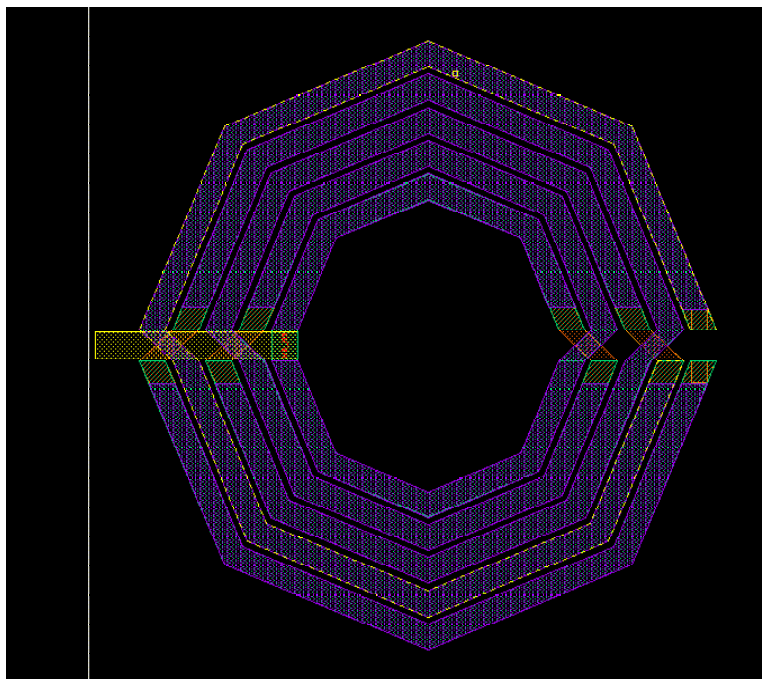


Figure 3: Layout of the Inductor using the Top Metal Layer (M4)

Results and conclusion:

The output from the VCO is shown in figure 4. The phase noise at 1MHz for an Oscillation frequency is shown in figure 5. The spectrum of the single-ended output is shown in figure 6. The VCO can be tuned from **1.4 GHz – 1.8 GHz** for a tuning range of **0-3.3 V**.

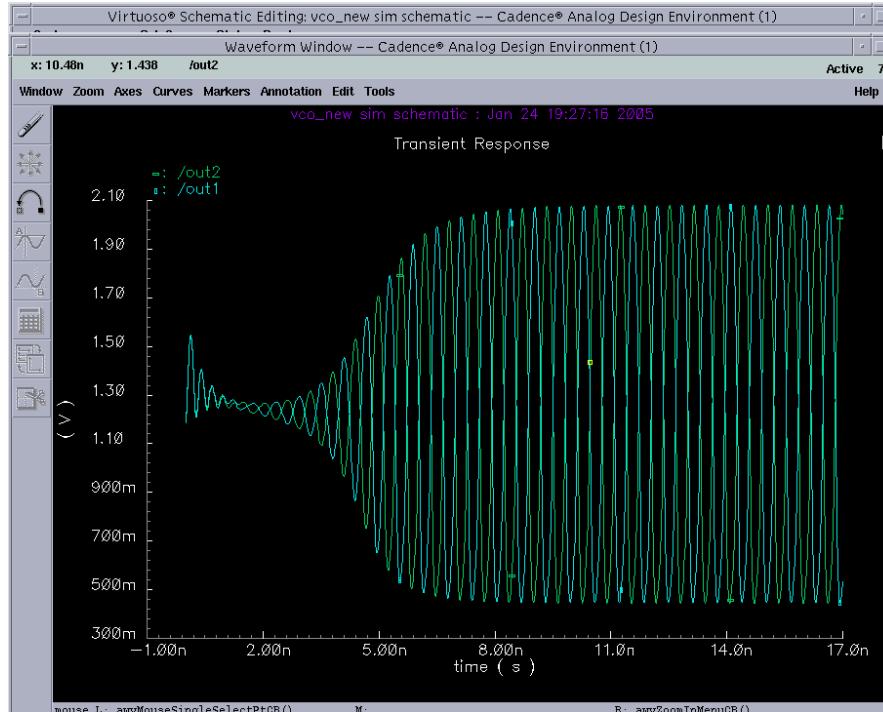


Figure 4: Output of the VCO

A differential buffer was used to drive the bond-pad, EDS and the package parasitics. The Package used was an LQFP-22 package. A PCB board was designed to test the VCO. Adequate Power supply filtering was provided on the PCB. The differential pair of the buffer was placed on-chip, whereas the biasing and load inductors were off-chip. Inductor loads were used to obtain higher swing. The output was monitored using an Agilent E4403B spectrum analyzer. The VCO's oscillation frequency was found to be 2.29 GHz for a control voltage of 3.3 volts. The output could be tuned from **1.85GHz – 2.29 GHz** for a control voltage of 0-3.3 V. The plot from the spectrum analyzer is shown in figure 7 and 8. The Output amplitude was much lesser than expected. This may be attributed to the Package parasitics.

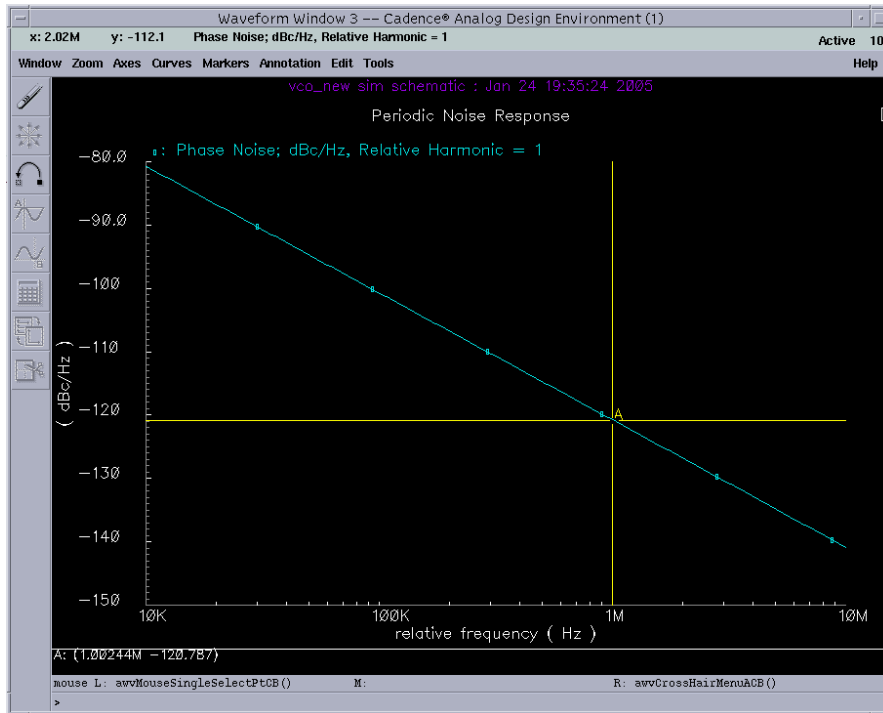


Figure 5: Phase noise of the VCO

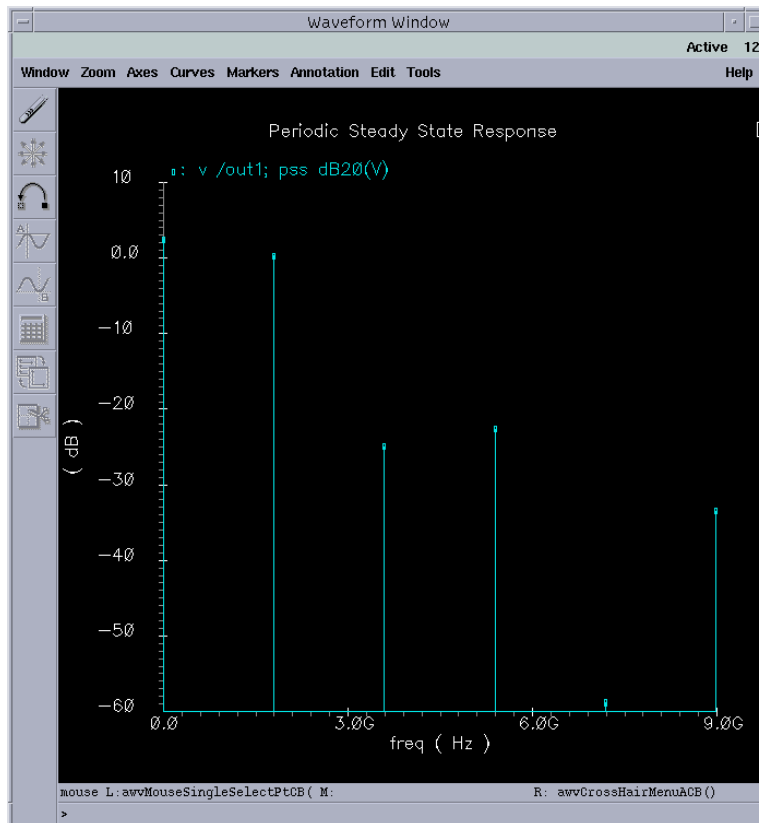


Figure 6: Single ended output spectrum

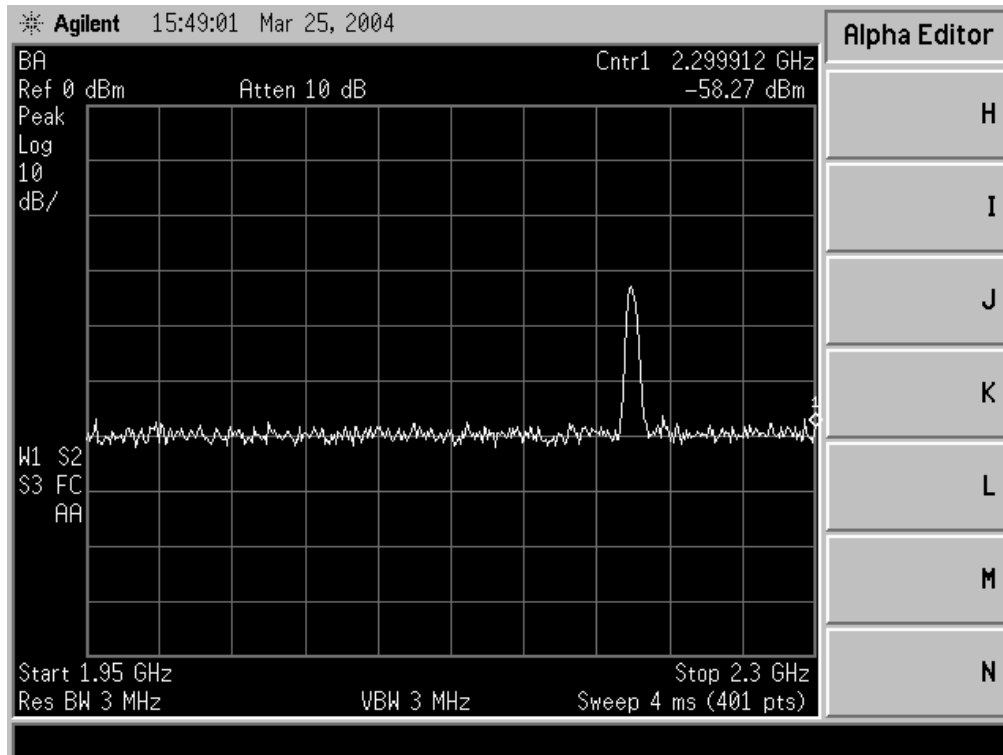


Figure 7: Plot from the spectrum analyzer

Conclusion:

The 1.8 GHz VCO employing On-chip inductors were successfully tested. The simulated tuning range was **1.4 GHz – 1.8 GHz** compared to tested tuning range of **1.85 GHz – 2.29 GHz**. This can be attributed to the modeling. The output was also severely attenuated. This can be due to the Package and the ESD diode capacitance. This project gave the authors and the other students of the Analog VLSI and Devices Lab, University of Tennessee a tremendous amount of exposure to RF VCO design. The Design experience from this design will be used to develop high performance VCOs in the days to follow.