

Design for MOSIS Educational Program (Research)

Analog Counter: (T42Q- AT)

Project Title

A CMOS Analog Counter employing Schmitt Trigger

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Working Principle of the Analog Counter

The block diagram of the analog counter is shown in Figure 1. The principle of operation of the Analog Counter is given below

- Current from current Generation circuit charges the capacitor C1 for a time interval given by an one-shot circuitry.
- The one-shot generates a pulse of a fixed-duration at the rising edge of each clock
- For each rising edge the capacitor is charged by Δv , until it reaches the switching point of the Schmitt trigger.
- The delay stages are needed to ensure that the capacitor starts at a zero voltage after counting the desired number of pulses.

The Analog Counter consists of three blocks. They are the Current-generating Circuit, one-shot and the Schmitt trigger. The one-shot produces pulses of fixed duration given by the values of R2, C2 and the switching point of the inverter INV1. The duration of the pulse dt is given by $R2.C2 \cdot \ln(V_{DD}/V_{DD}-V_{SW})$. The reversed biased diode at the input of the inverter fixes the node at 5V (VDD) if the charge across the capacitor exceeds 5v.R2 and C2 determine the frequency of the input signal for which the one-shot can produce the output of the right width. Figure 2 gives the schematic of the one-shot

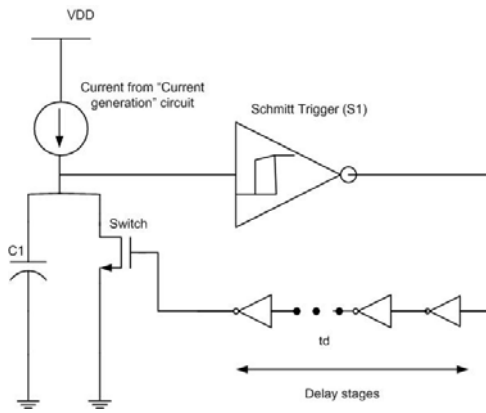


Figure 1:Block Diagram of the Counter

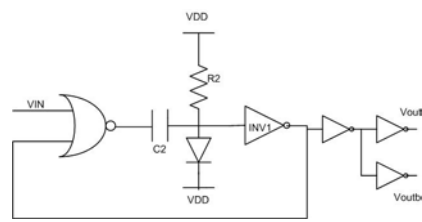


Figure 2: Block Diagram of the One-shot

The current that charges the capacitor is generated as shown in figure 3. A high-swing cascode configuration is used to mirror the current accurately. The op-amp is a folded cascode op-amp that has a very high DC gain.

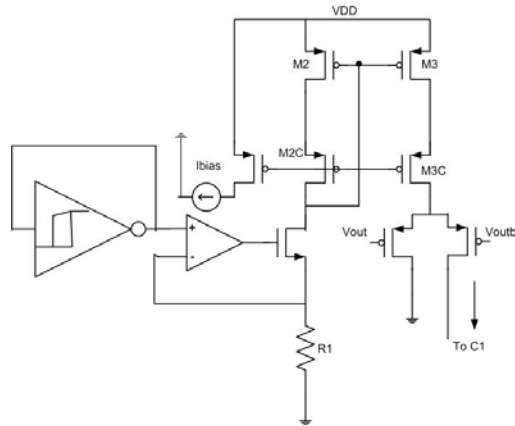


Figure 3: Block Diagram of the Current Generation Circuit

Derivation of the Count N:

$$\Delta V = \frac{I}{C1} * \Delta t$$

ΔV – Change in voltage across the capacitor
 I – Current from the current generation circuit
 Δt – Duration of the pulse from the one-shot

$$\Delta t = R2.C2.\ln\left(\frac{VDD}{VDD-VSP}\right) \quad , \text{ VSP is the switching point of INV1}$$

$$I = \frac{VSWM + VOS}{R1} \quad , \text{ VSM is the switching point of S1 with in and out shorted}$$

Therefore,

$$\Delta V = \frac{VSWM + VOS}{R1 * C1} * R2C2 \ln\left(\frac{VDD}{VDD-VSP}\right)$$

The count is given by,

$$N = \frac{VSWH}{\Delta V} = \left(\frac{VSWH}{VSWM}\right) * \frac{R1C1}{R2C2.\ln(VDD / VDD - VSP)}$$

VSP is the switching point of the inverter used in the one-shot
VSWH is the switch point of the Schmitt Trigger when switching from high to low.

Measurement and Characterization results of the Analog Counter fabricated using AMI-.5u CMOS process:

The Counter was designed to give a count of 8. The following were the circuits that were fabricated through MOSIS.

1. The analog counter System
2. The oneshot
3. Schmitt-Trigger
4. Inverter
5. Opamp

The circuits were tested in the Analog VLSI and Devices Laboratory at the University of Tennessee and the test results were compared with the simulation results. The test and measurement results of the individual blocks are given below

Schmitt Trigger:

The measured results for the Schmitt trigger are shown in figure 4.

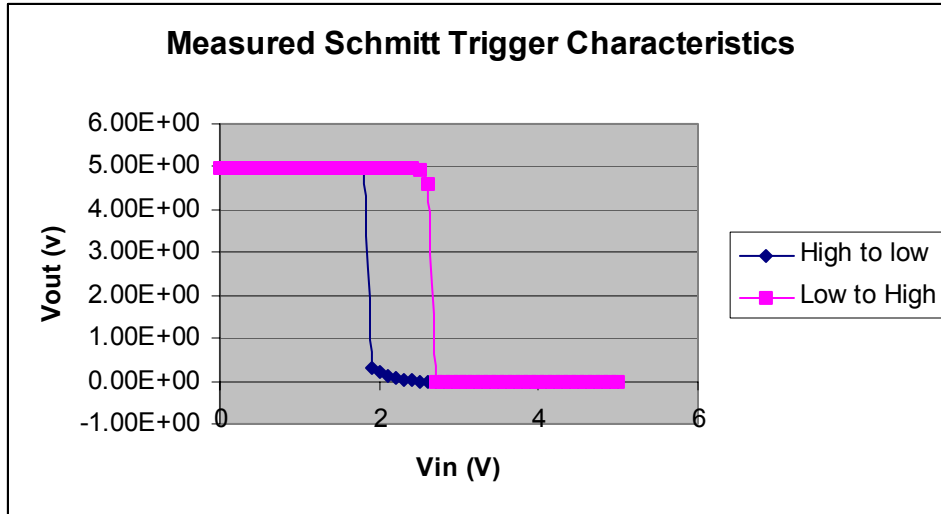


Figure 4: Measured Schmitt Trigger Characteristics

Table 1 compares the measured and the simulated high and low switching points

Switching Point	Simulated	Measured
VSWH	2.5	2.53
VSWL	1.98	1.93

Table 1: Measured VS Simulated Schmitt Trigger Characteristics

Inverter:

The measured result for the inverter is shown in figure 5.

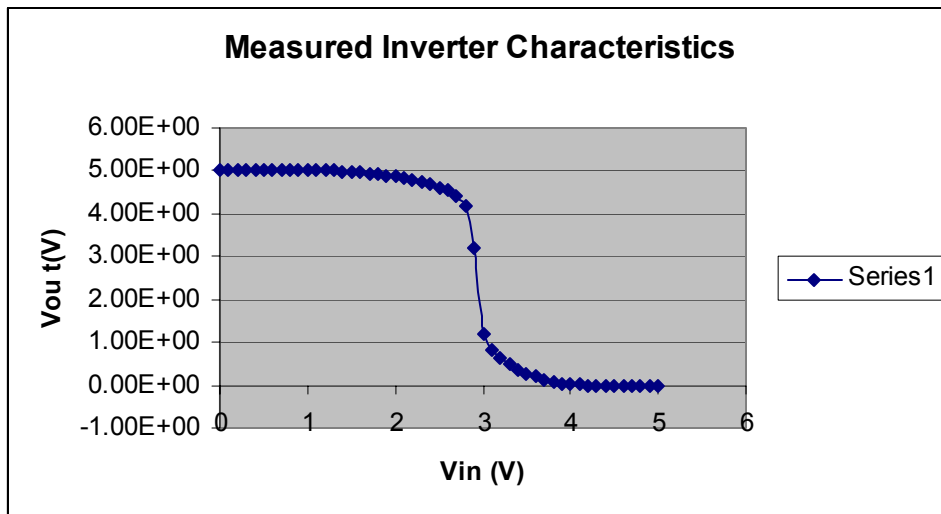


Figure 5: Measured inverter Characteristics

Table 2 compares the measured and the simulated switching point of the inverter

Switching Point	Simulated	Measured
Vsp	2.83	2.8

Table 2: Measured VS Simulated Inverter switching points

Operational-Transconductance Amplifier

The OTA was a folded-cascode OTA that has a simulated gain of 70 DB. The following measurement results were obtained from the OTA.

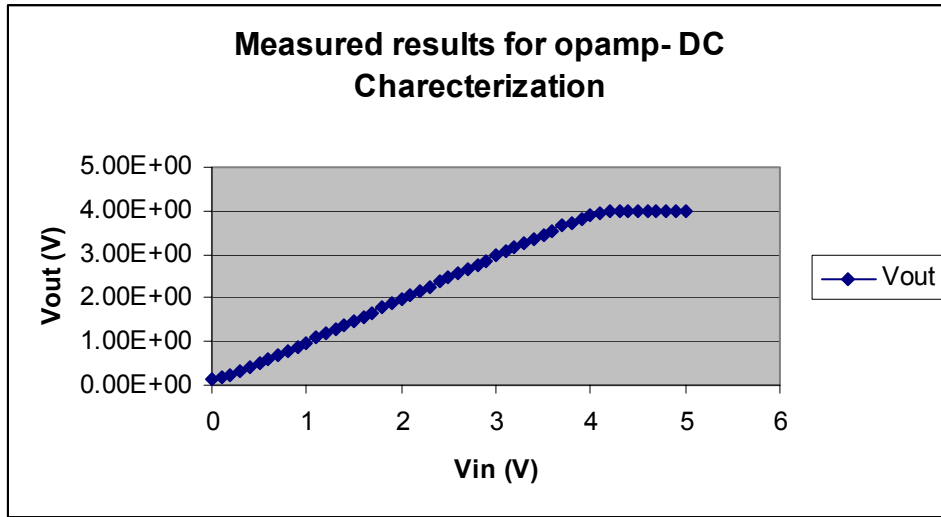


Figure 6: DC sweep with the OTA as a Voltage follower

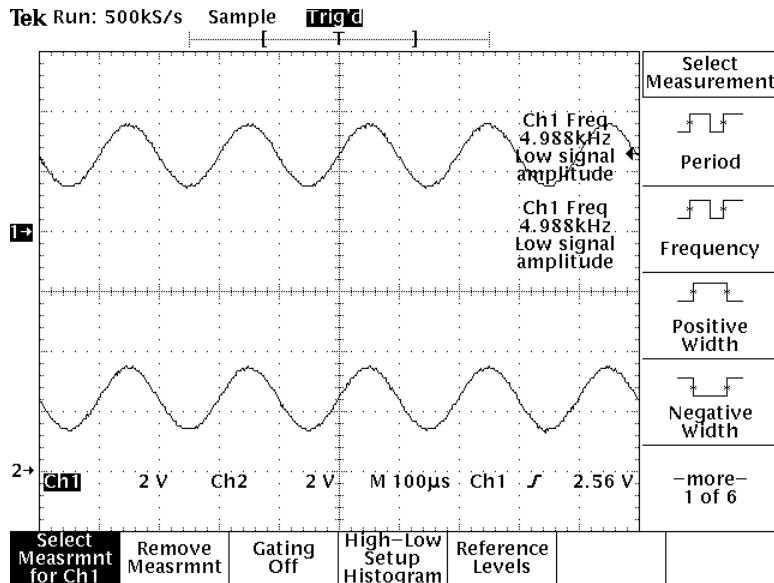


Figure 7: Voltage follower setup with a low frequency sine wave as the input

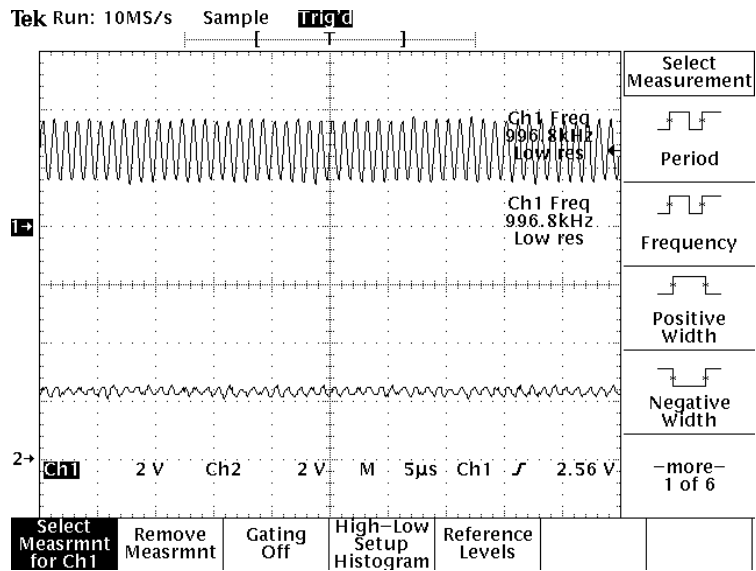


Figure 8: Voltage follower setup with a high frequency sine wave as the input

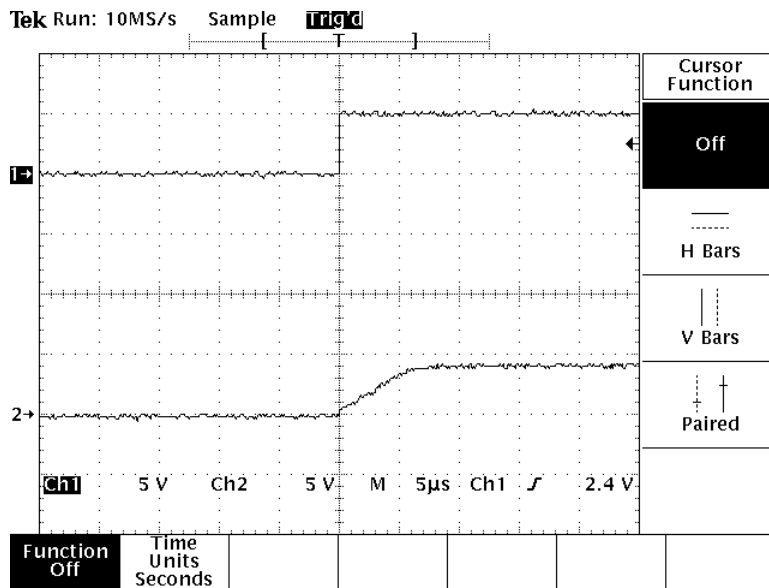


Figure 9: Slewing of the OTA

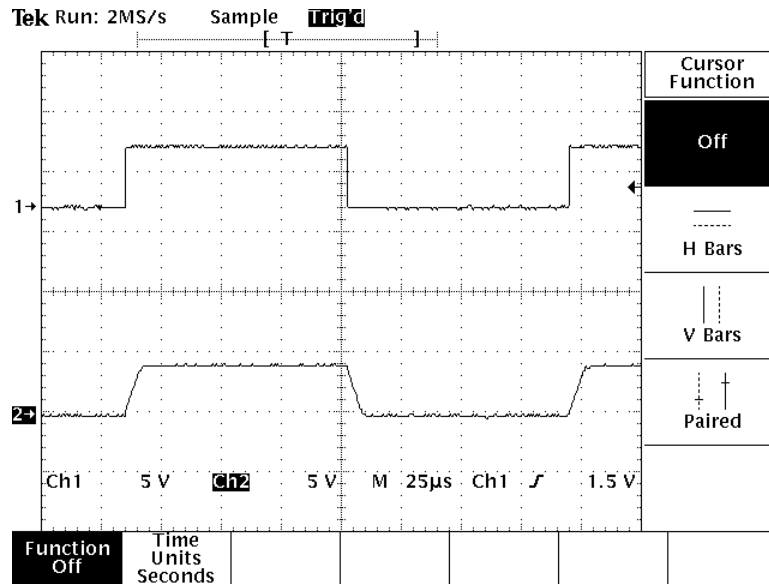


Figure 10: Positive and Negative Slewing of the OTA

The measured results from the OTA that are of importance here are tabulated below in table 4 . The load capacitance is 20pF. The bias current is 20uA.

Gain	72 DB
Offset	2mV
Slew-Rate +ve	1v/uS
Slew-Rate -ve	1v/uS
UGF	500 KHZ
Common-Mode Range	0V – 4V

Table 4: Measured Results for the OTA

The simulated results for a current of 20uA and a load capacitance of 5pF are shown in table 4.

Gain	70 DB
Offset	50uV (random offset are not shown in simulation)
Slew-Rate +ve	5 v/uS
Slew-Rate -ve	5 v/uS
UGF	2 MHZ
Common-Mode Range	0V – 4V

One-Shot:

The One-shot failed to work. The Capacitor was measure to be about 220fF and the intended value was 200Ff. The resistor is 40K. This gives a pulse width of about 7ns. Since the pulse width is two narrow it might have been attenuated by the parasitics of the package.

Analog Counter System:

The failure of the one-shot may have caused the whole counter system to malfunction. The counter system will be redesigned after making the modifications to the One-shot. The new design of the One-shot will have a wider pulse generated by increasing R and C.

Conclusion:

The operation principle of the Analog Counter was given and the equation of the count was derived. The simulation and the test results of the individual working blocks of the counter were given. The failure of the system is attributed to the failure of the One-shot. The One-shot design will be rectified and the design will be resubmitted.